

MODEL NAME : *PALB0*
PCB NO : *LA-6801P (DAB00000400)*
BOM P/N : *46198531L01*
46198531L02

Dell/Compal Confidential

Schematic Document

Specter (Huron River)

Sandy Bridge (PGA) + Cougar Point (standard)

DISCRETE VGA N12E-GE-B (optimus)

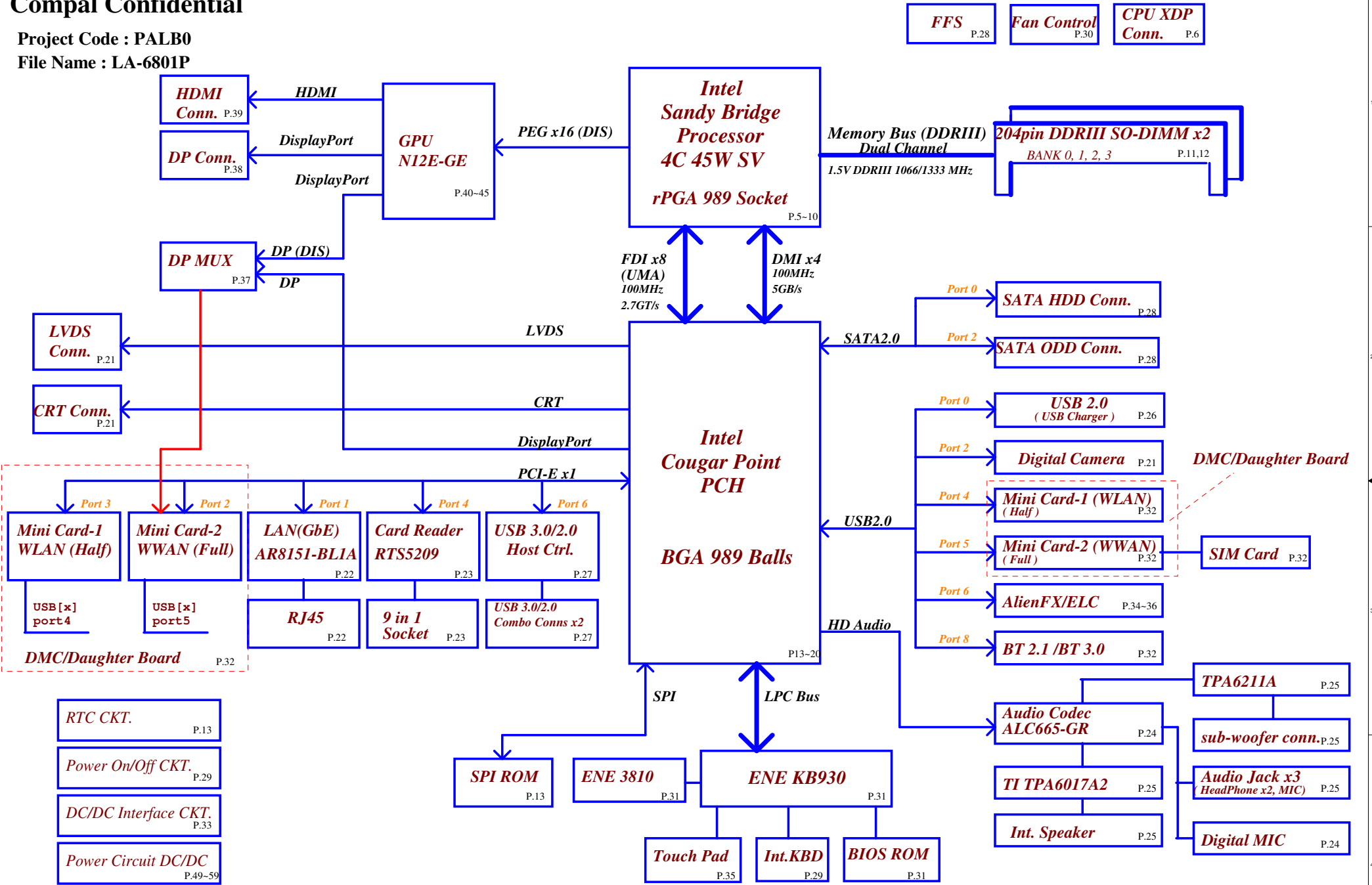
2010-12-06

Rev: 0.3

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Issued Date	2010/12/01	Deciphered Date	2011/12/01	Title	Cover Page
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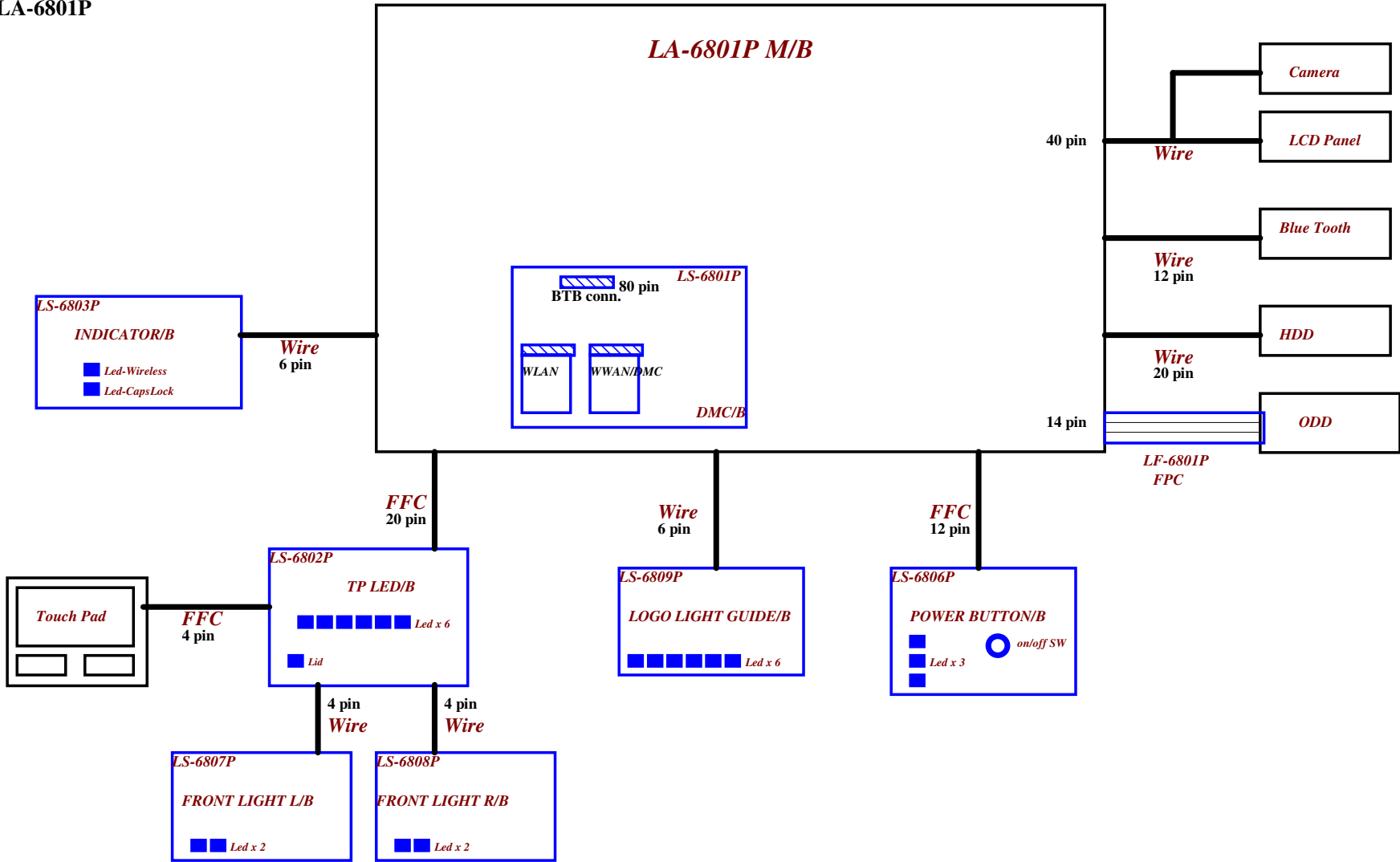
Project Code : PALB0
File Name : LA-6801P



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Project Code : PALB0
File Name : LA-6801P



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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Thermal Sensor 1	Thermal Sensor 2	FFS	VGA Thermal Sensor	VGA	DMC	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB930			V									
EC_SMB_CK2 EC_SMB_DA2	KB930					V	V		V				
PCH_SML0CLK PCH_SML0DATA	PCH												
PCH_SML1CLK PCH_SML1DATA	PCH												V
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V			V		V	V	V	

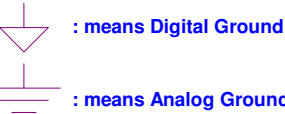
Link

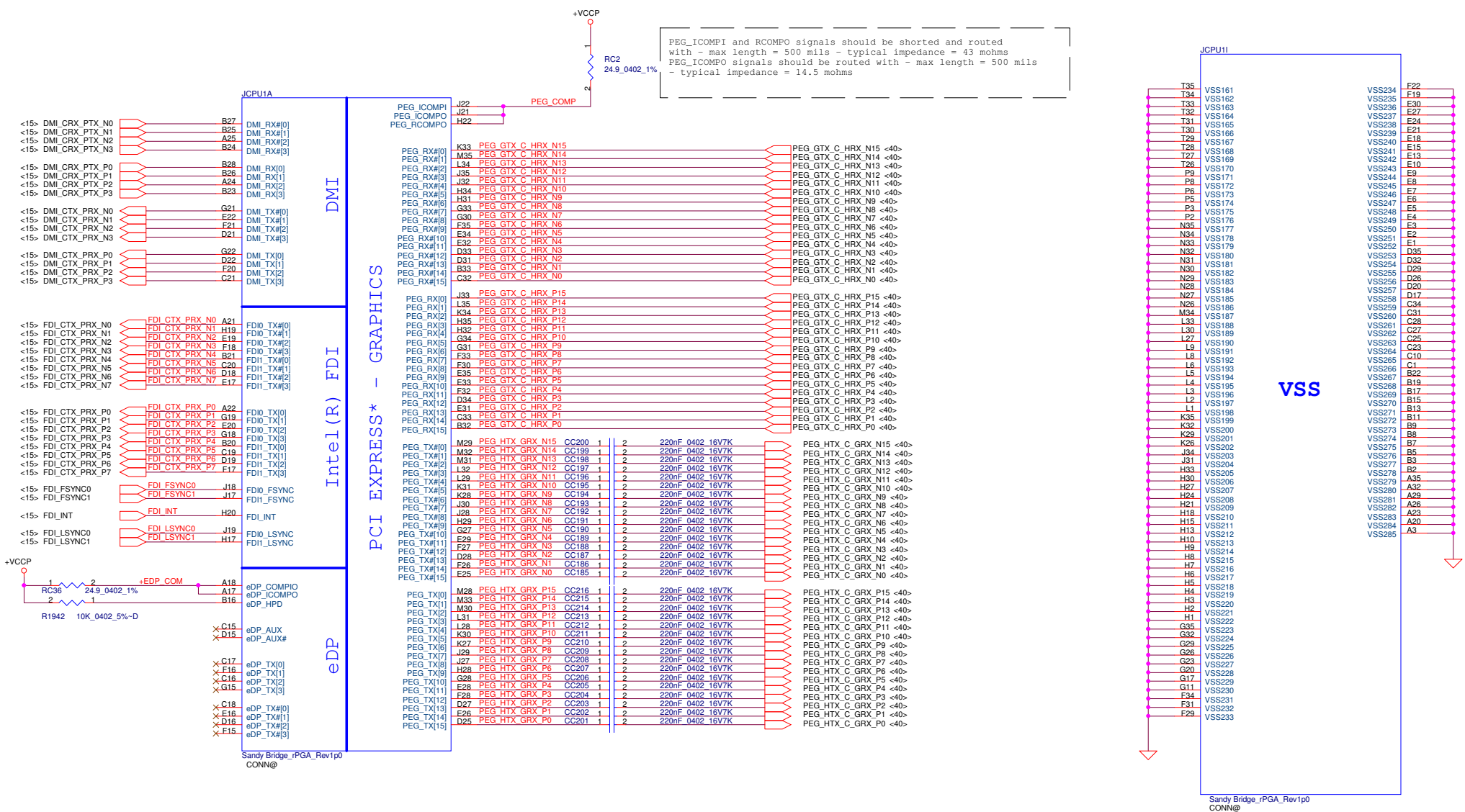
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

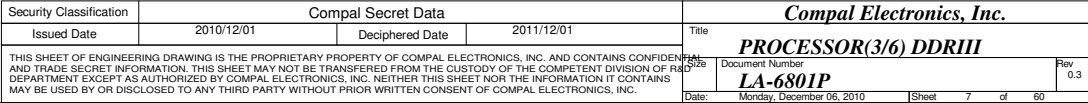
SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

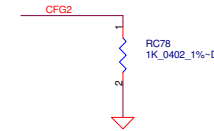
Symbol Note :



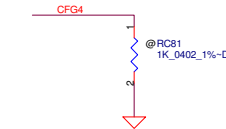




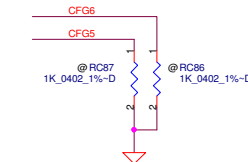
CFG Straps for Processor



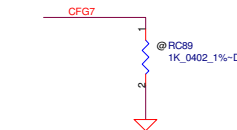
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition *0: Lane Reversed



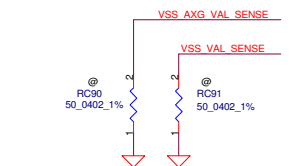
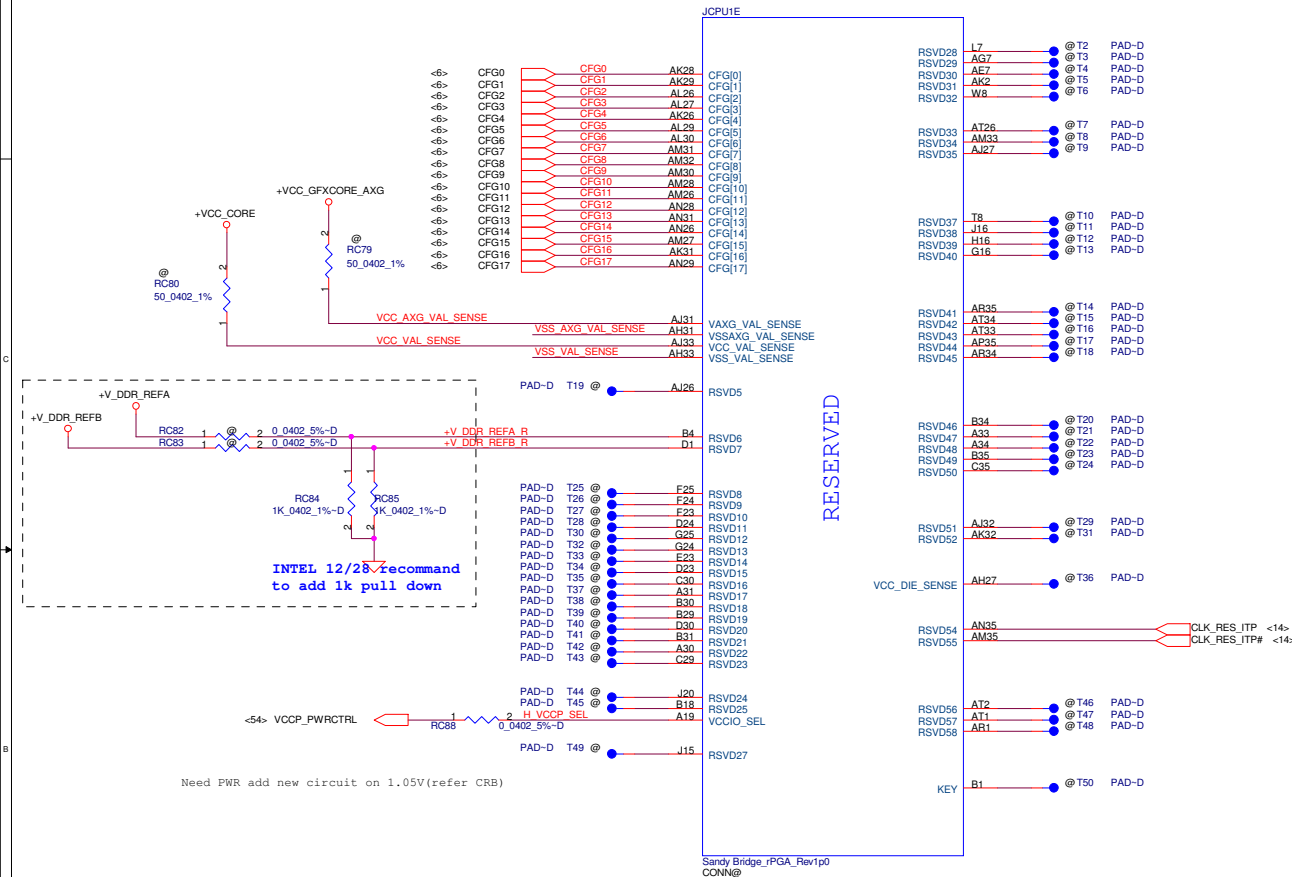
Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	*1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



INTEL 12/28 recommend
to add RC120, RC121, RC122, RC123
Please place as close as JCPU1

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				PROCESSOR(4/6) RSVD,CFG	
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JCPU1F

QC=94A
DC=53A

8.5A PDDG 0.7@P12

PEG AND DDR

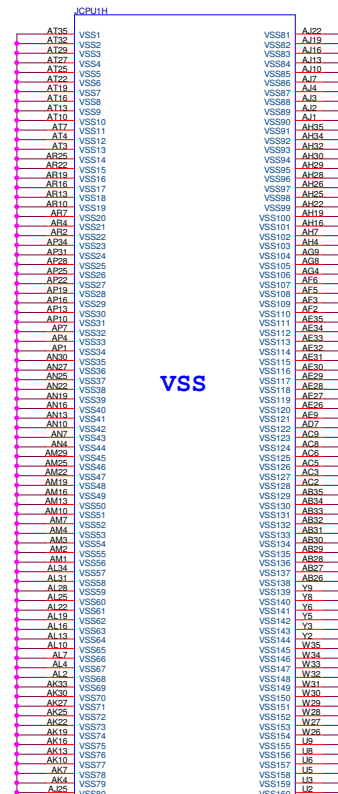
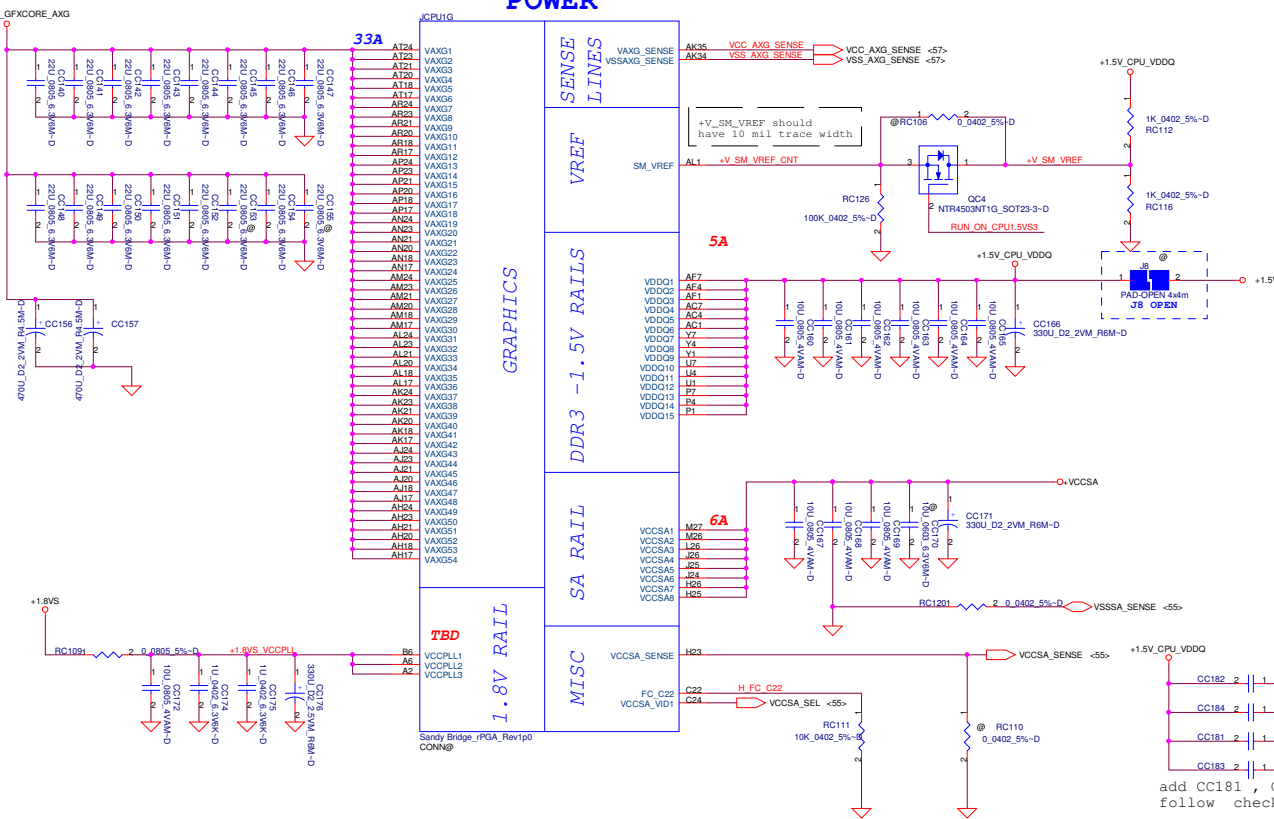
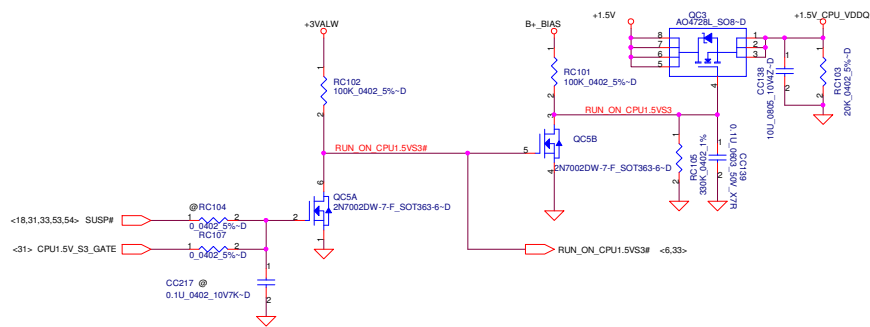
CORE SUPPLY

SVID

SENSE LINES

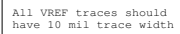
Sandy Bridge_rPGA_Rev1p0
CONN@

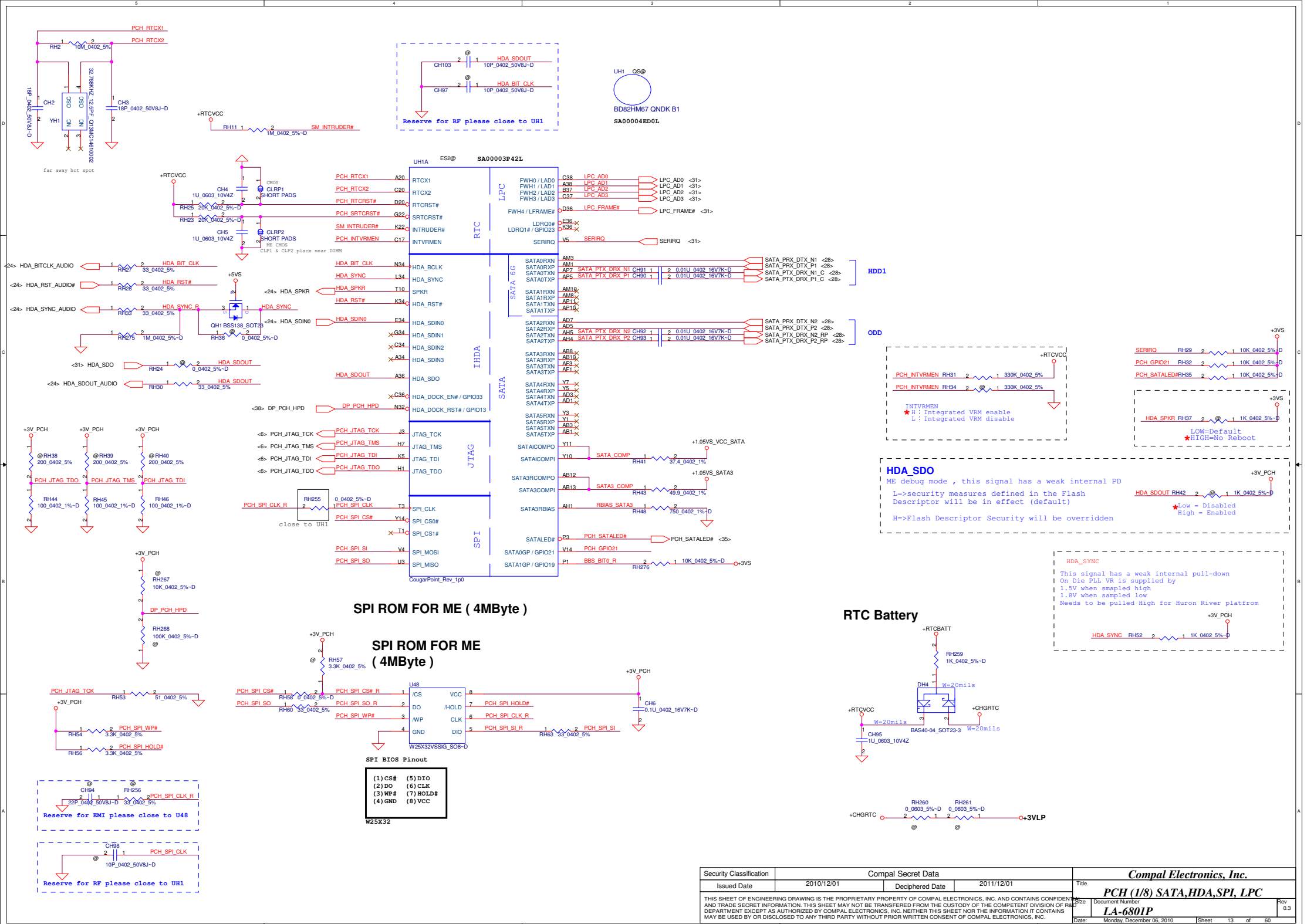
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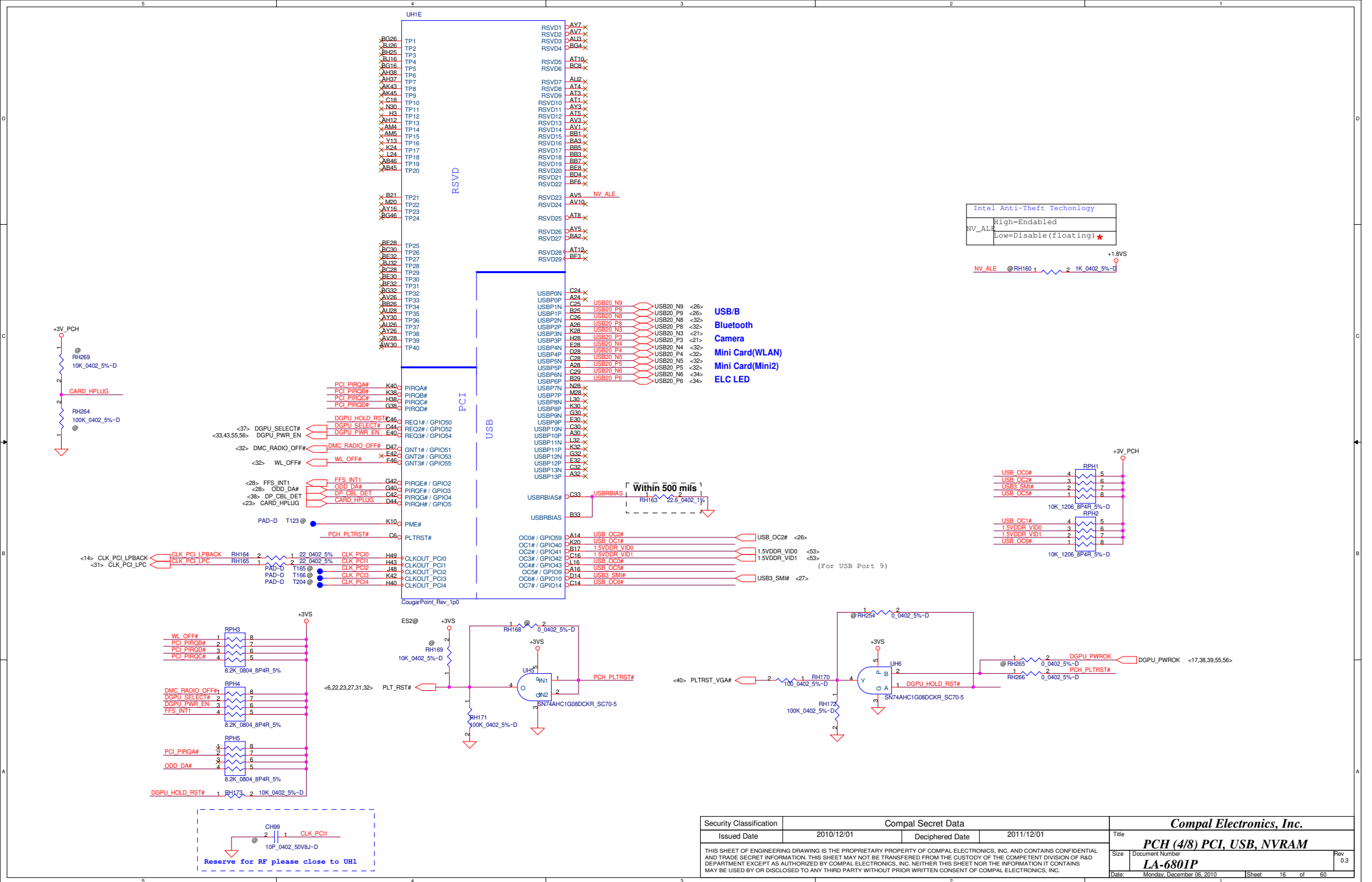
add CC181 , CC182, 4 caps are all pop.
follow checklist 1.0 5/24

Security Classification	Compal Secret Data		Compal Electronics, Inc. PROCESSOR(6/6) PWR,VSS	
Issued Date	2011/2/01	Deciphered Date	2011/2/01	Title PROCESSOR(6/6) PWR,VSS Docu. No. LA-6801P
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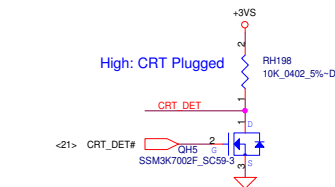
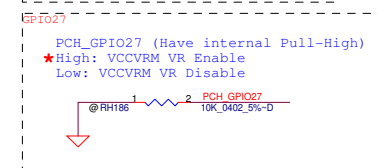
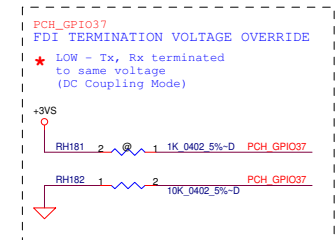
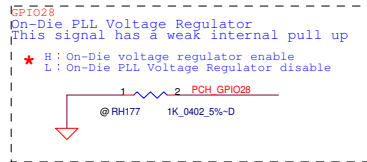
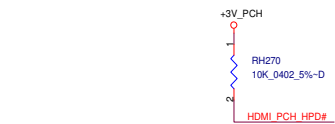




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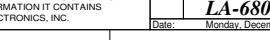
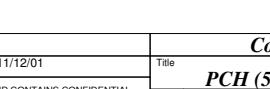
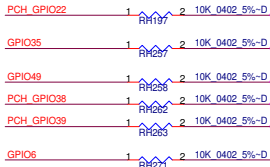
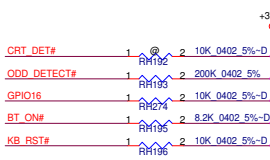
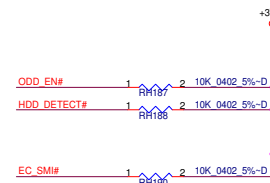
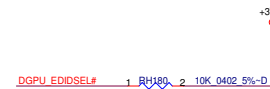
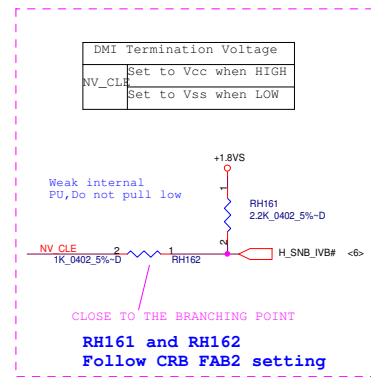
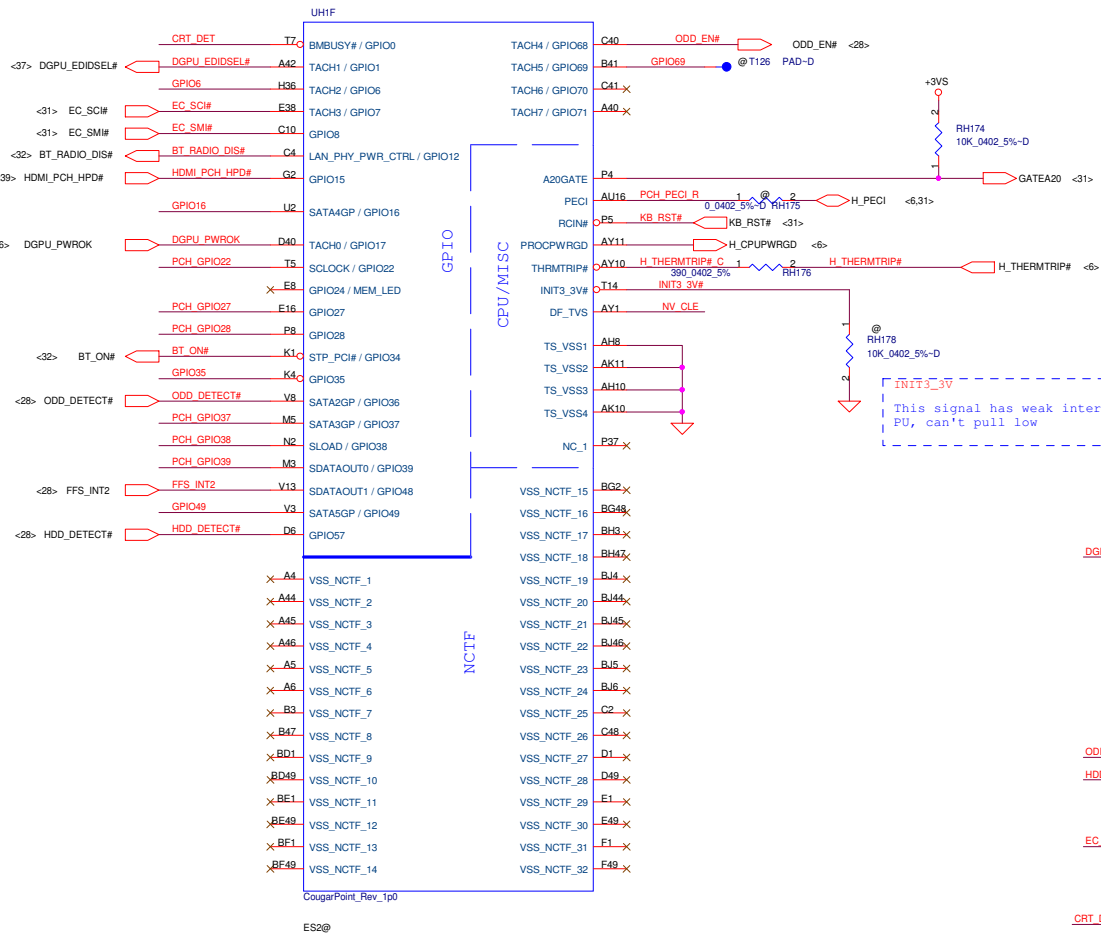


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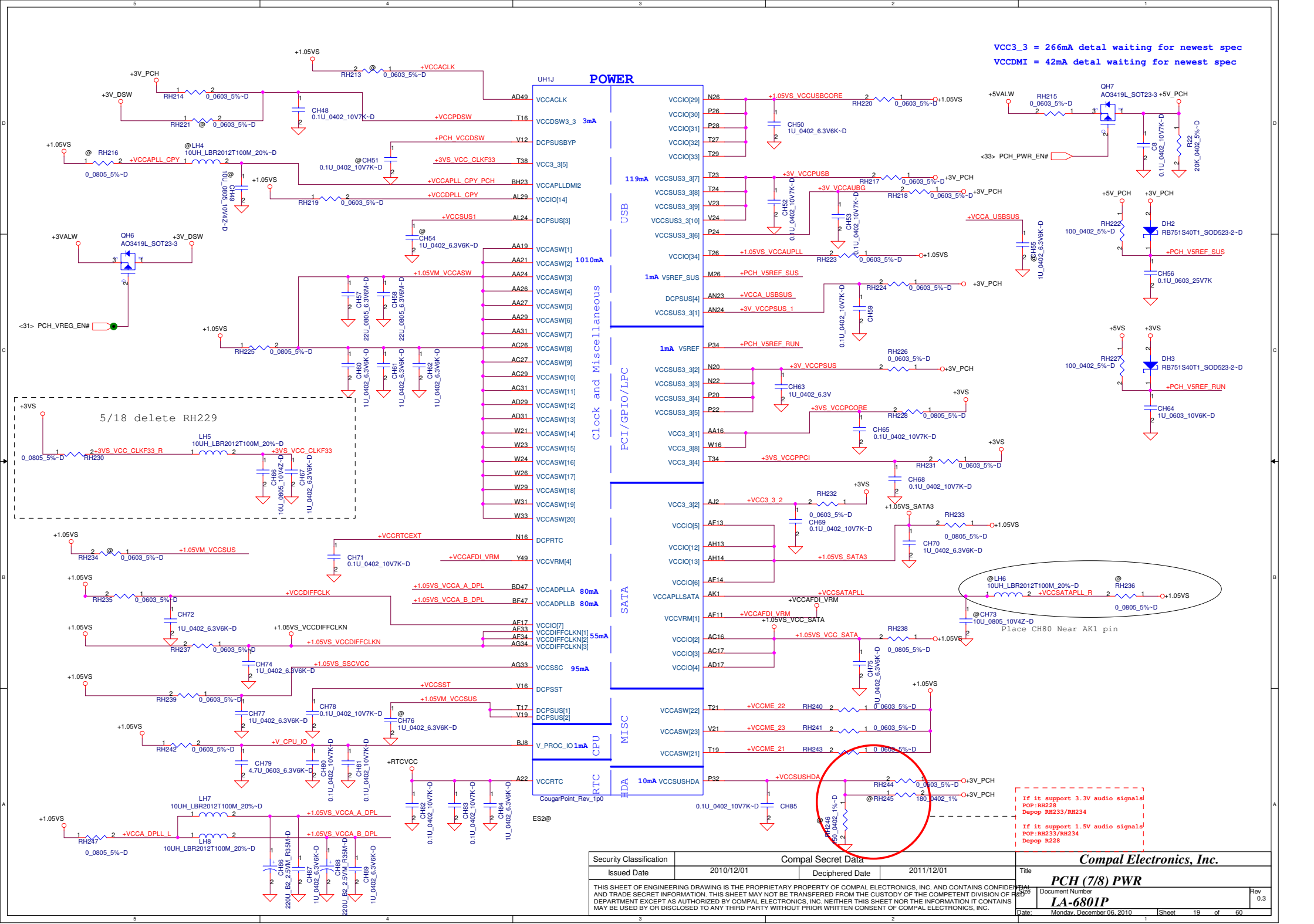


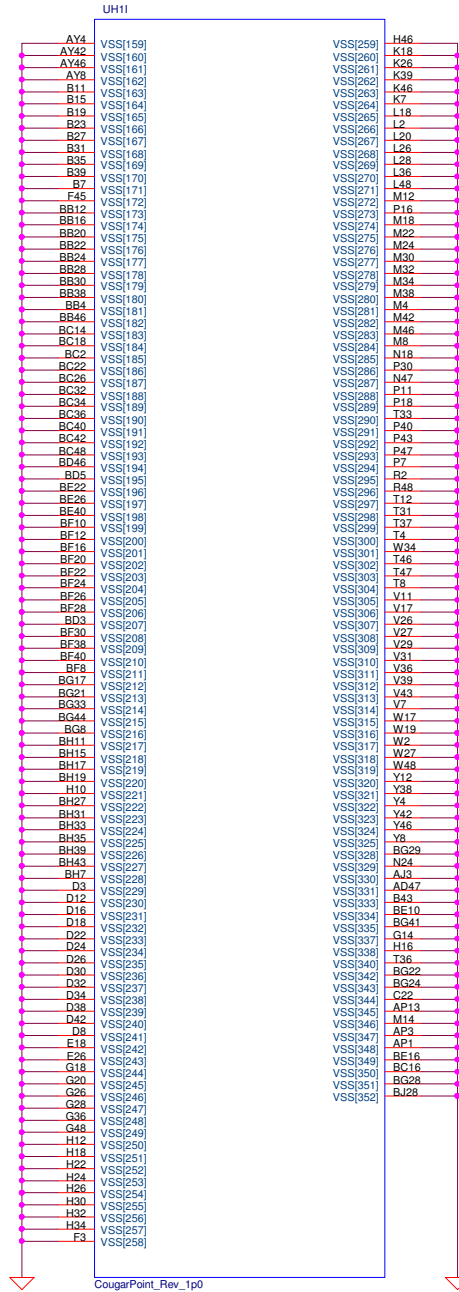
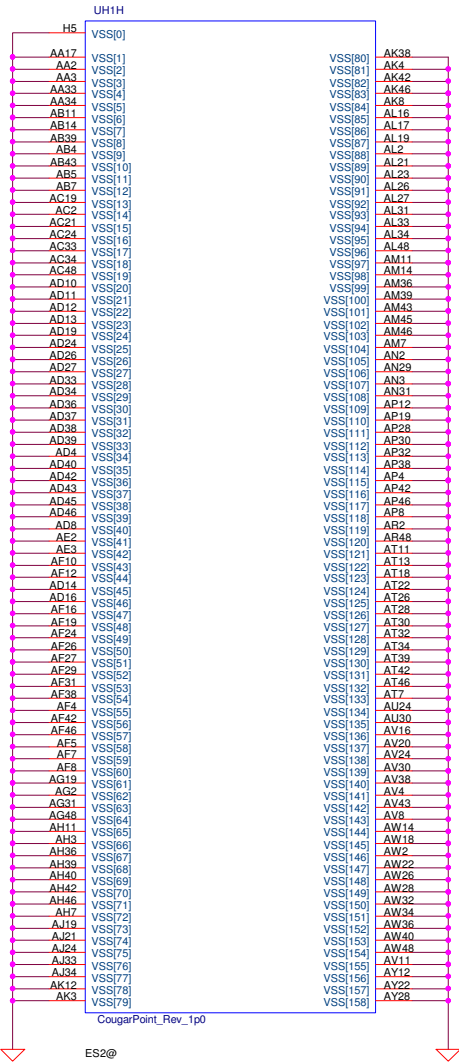
PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16

Please refer to Huron River Debug Board DG 0.5

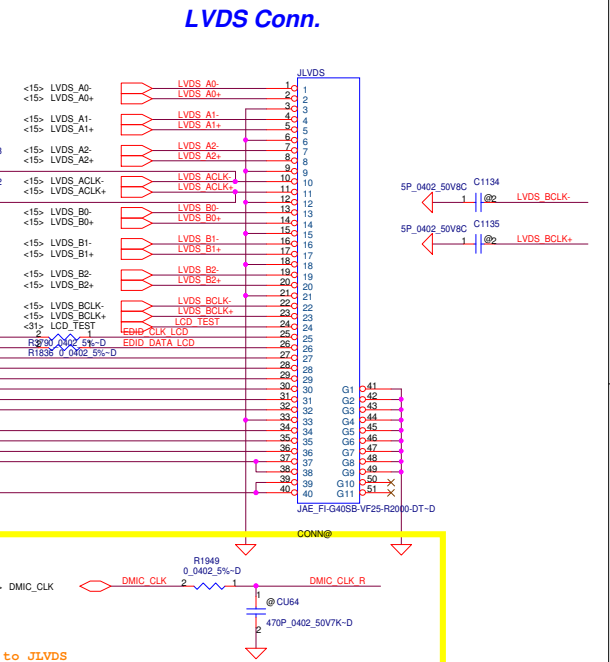
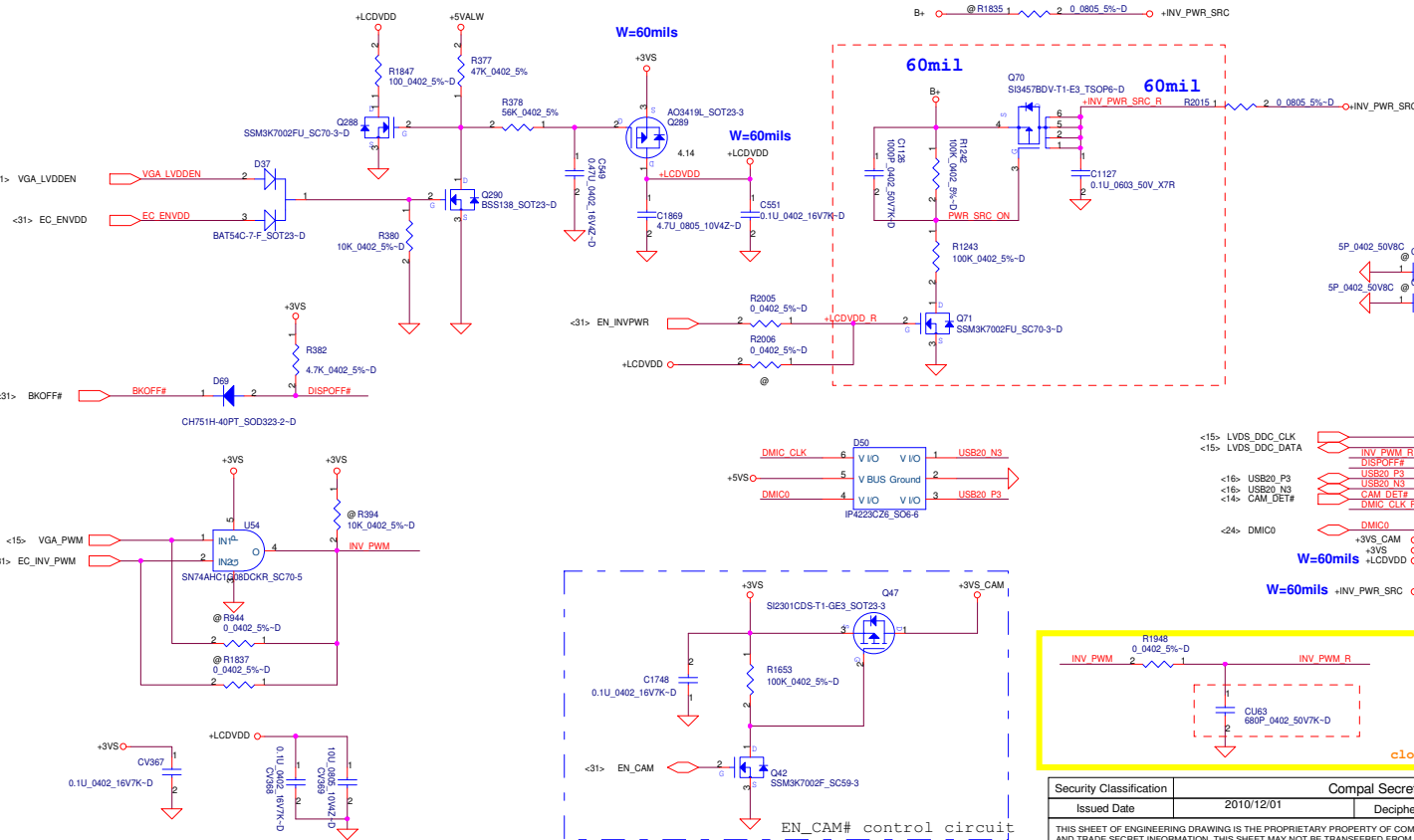
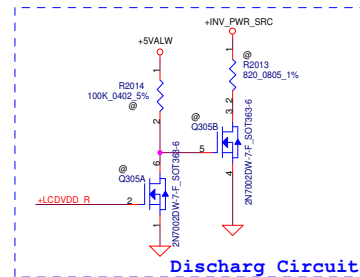
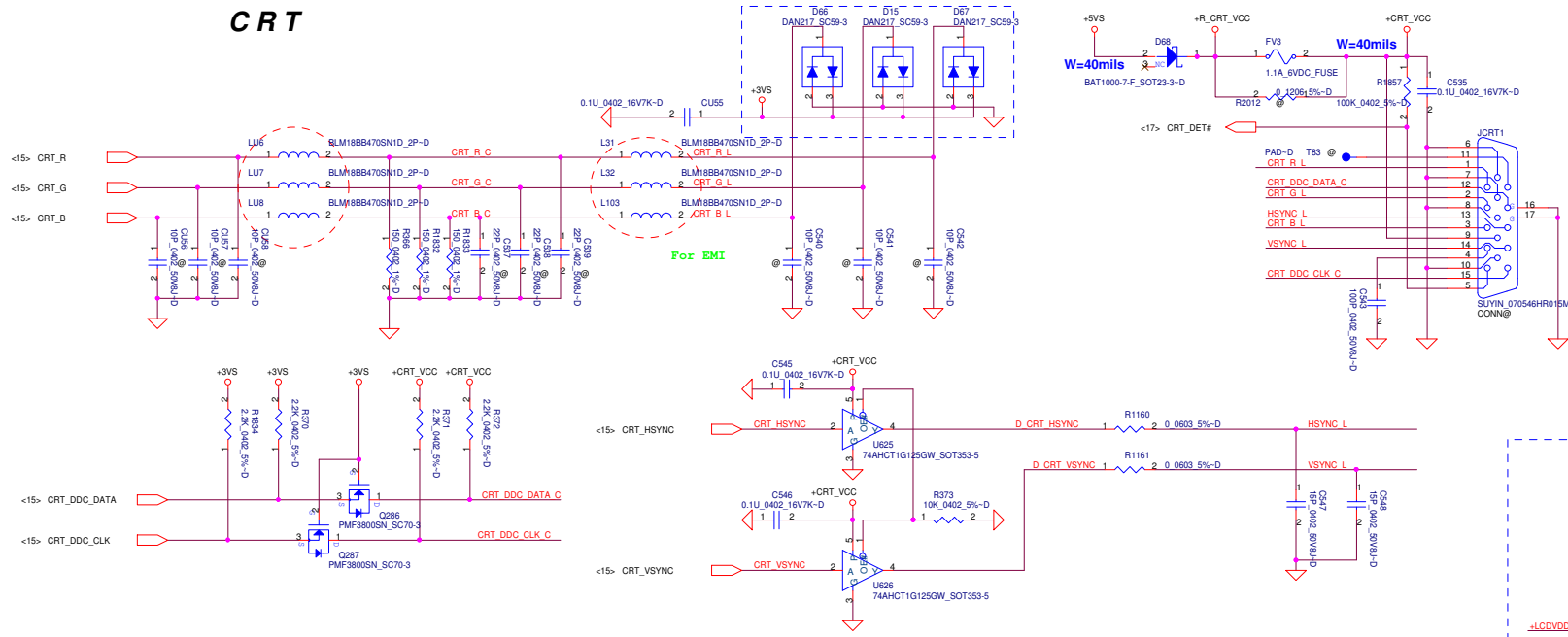


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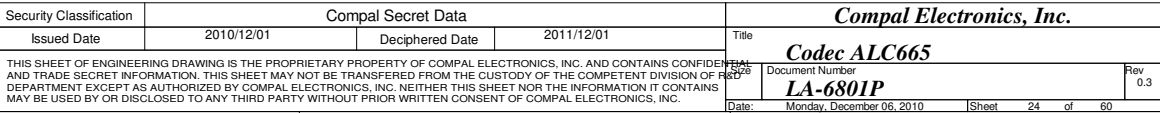




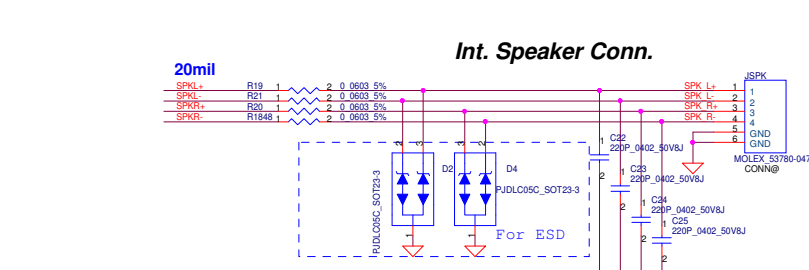
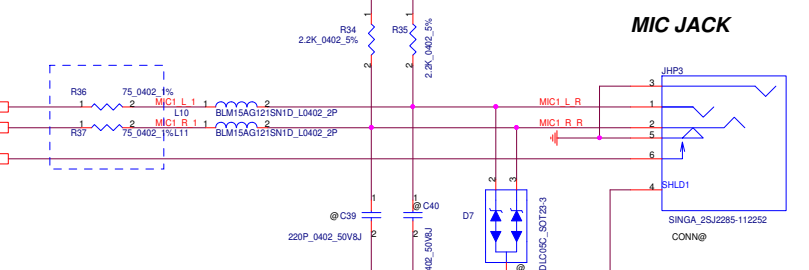
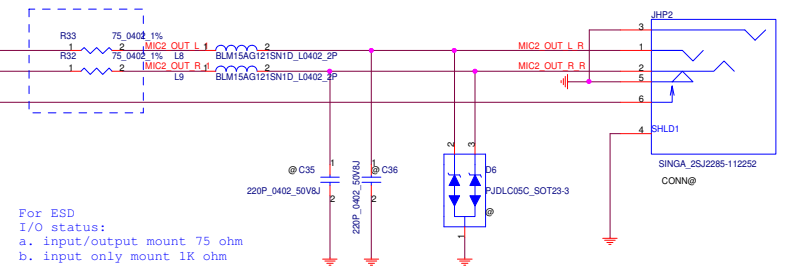
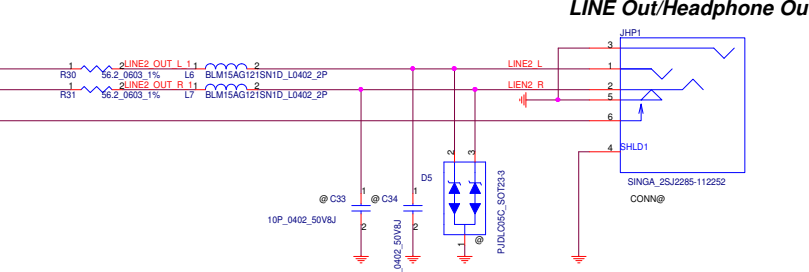
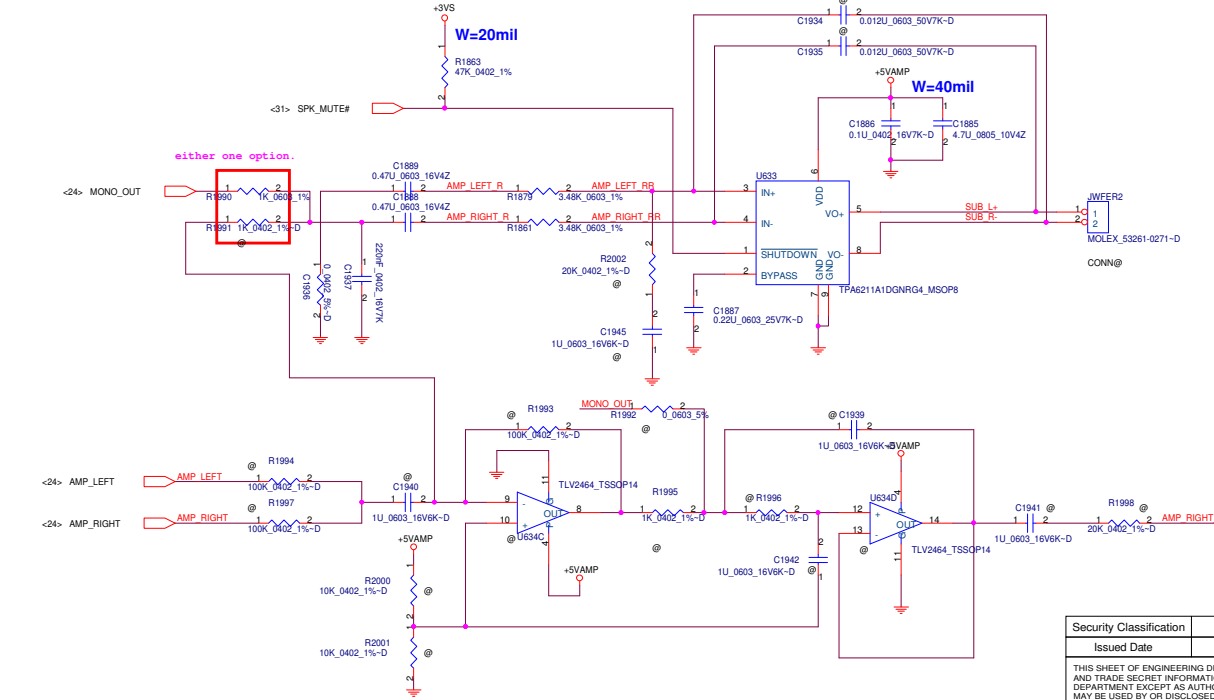
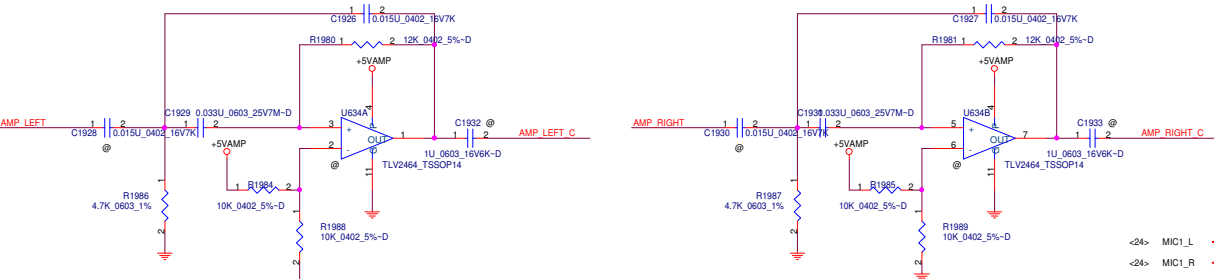
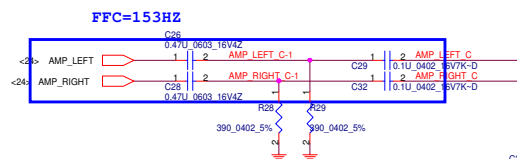
CRT



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						VGA / LVDS /camera conn.				
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									EA-6801P	0.3
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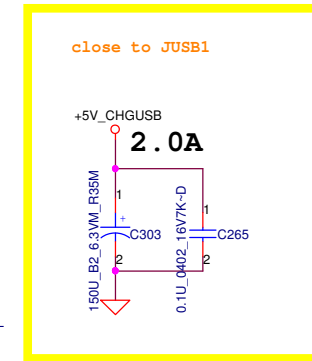
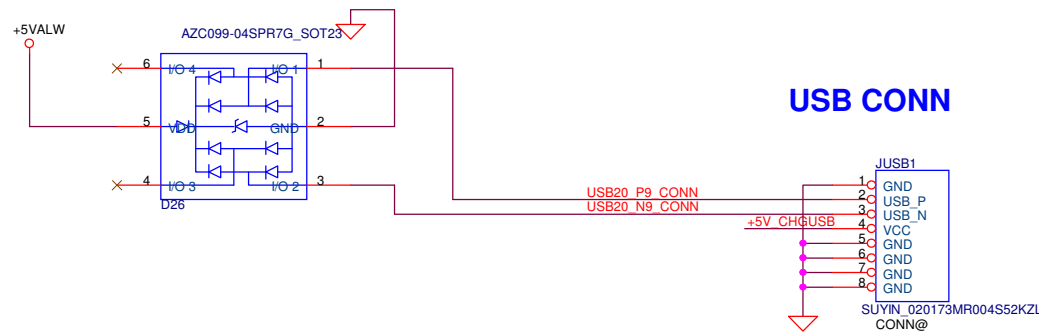
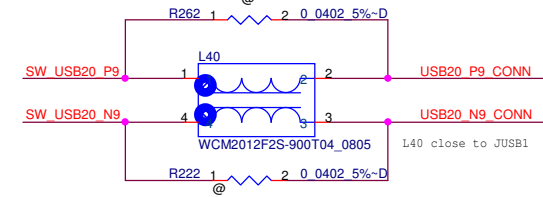
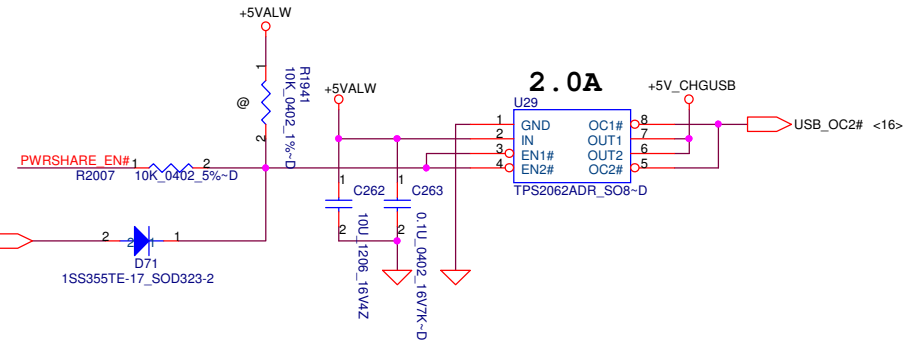
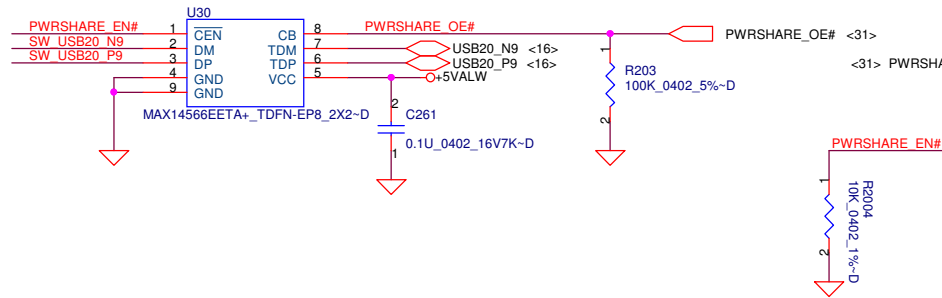


GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

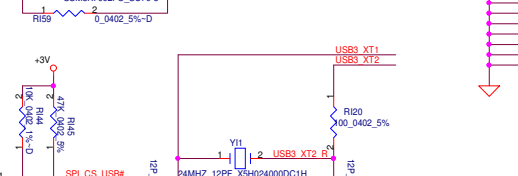
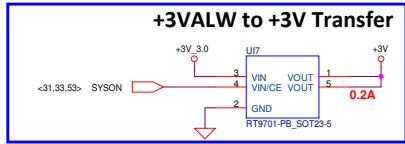


Power share

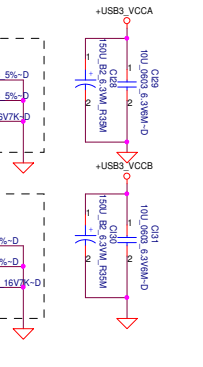
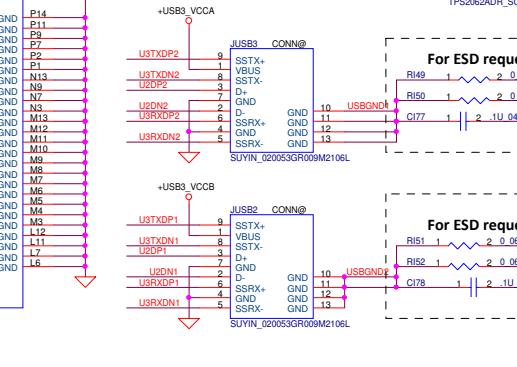
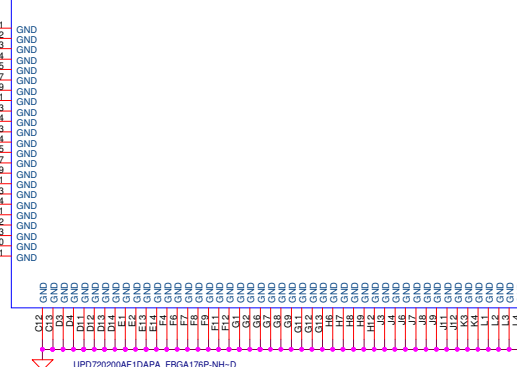
CB	Function
L	auto detection charger identification active
H	DP/DM=TDP/TDM

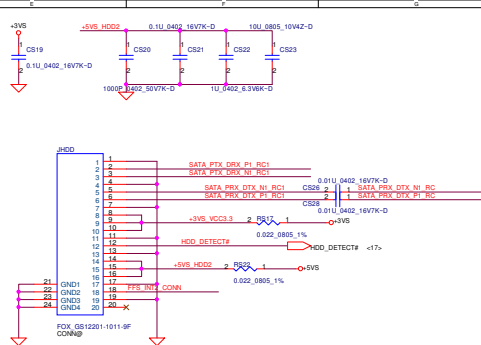


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Issued Date	2010/12/01	Deciphered Date	2011/12/01	Title	USB conn.	
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	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25





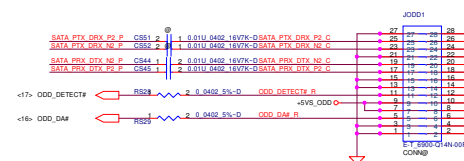
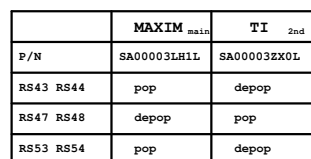
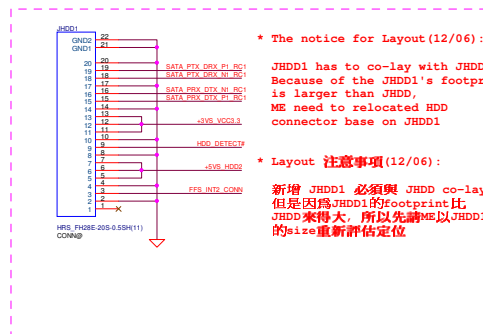
FFS_INT1 connect to PCN_GP120 & EC
discuss with BIOS to use which pin

<16> FFS_INT1 FFS_INT1
<17> FFS_INT1 FFS_INT1

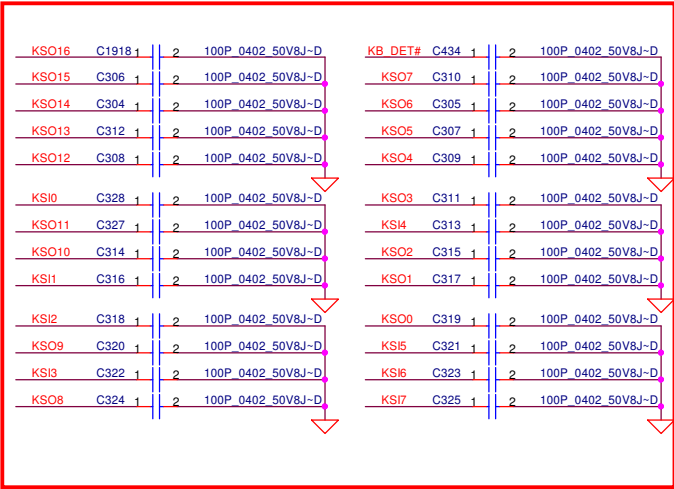
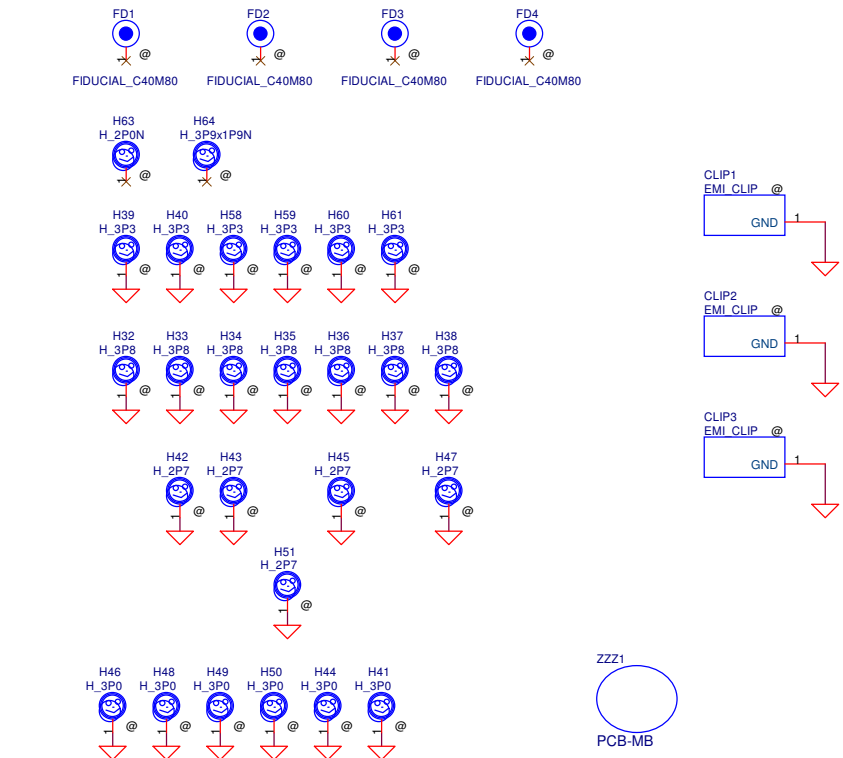
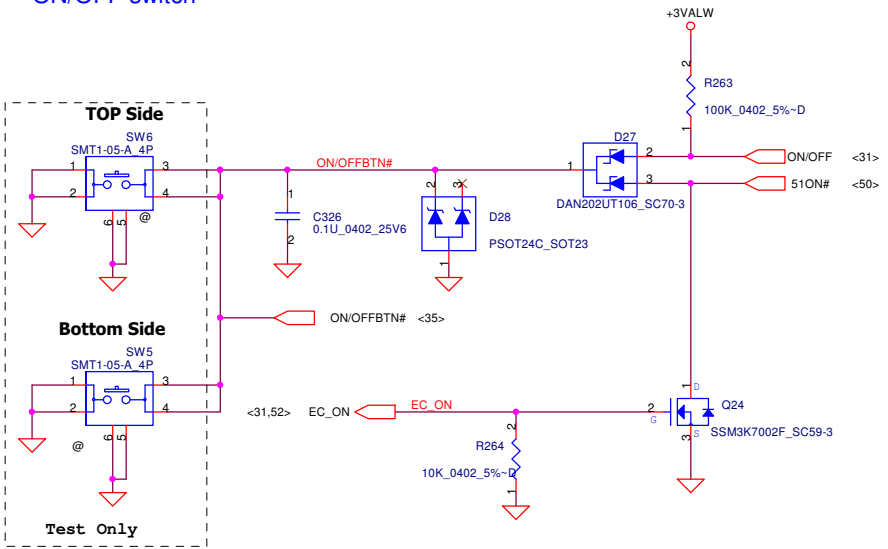
<6,11,12,14,32> PCN_SMIDATA
<6,11,12,14,32> PCN_SMBCLK

U18
DE35151DR

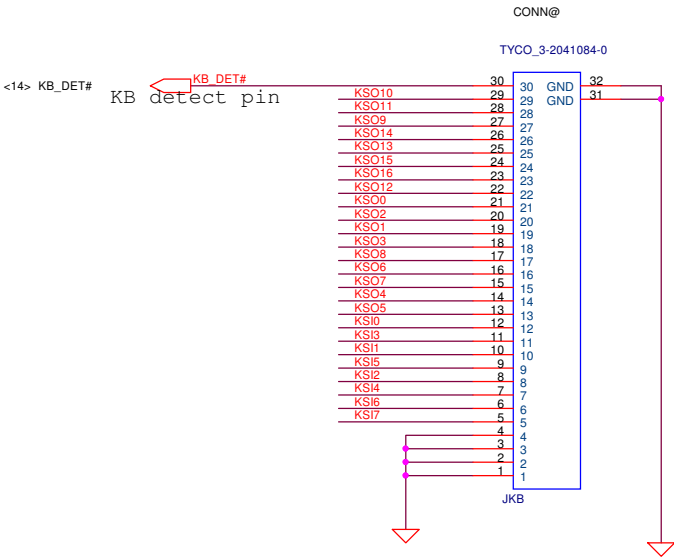
VDD IO
GND
AT1
AT2
SDD
SSA/SDI/SDO
SCL/SFC
RSTV
CS
+5V
DE35151DR_VDDIO_5V3



ON/OFF switch Power Button

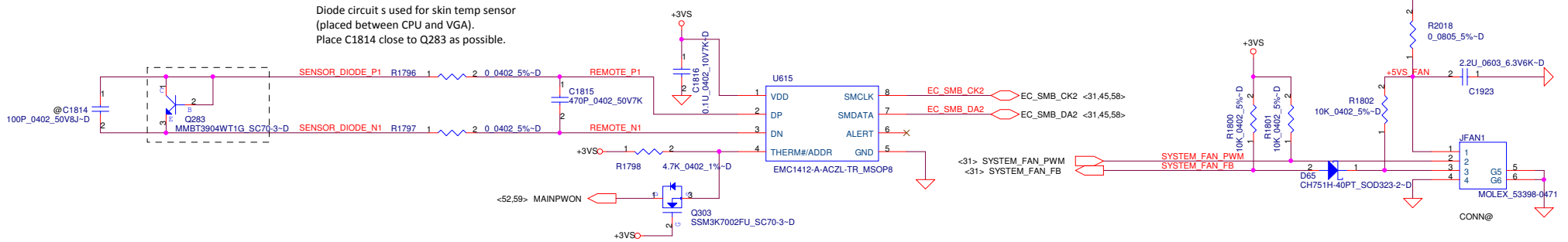


INT_KBD Conn.



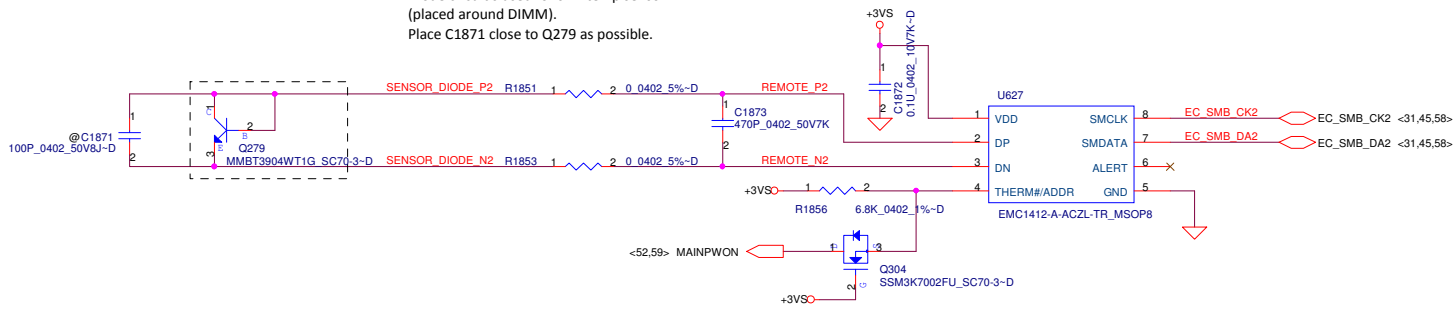
System Thermal Sensor 1

Diode circuit s used for skin temp sensor
(placed between CPU and VGA).
Place C1814 close to Q283 as possible.

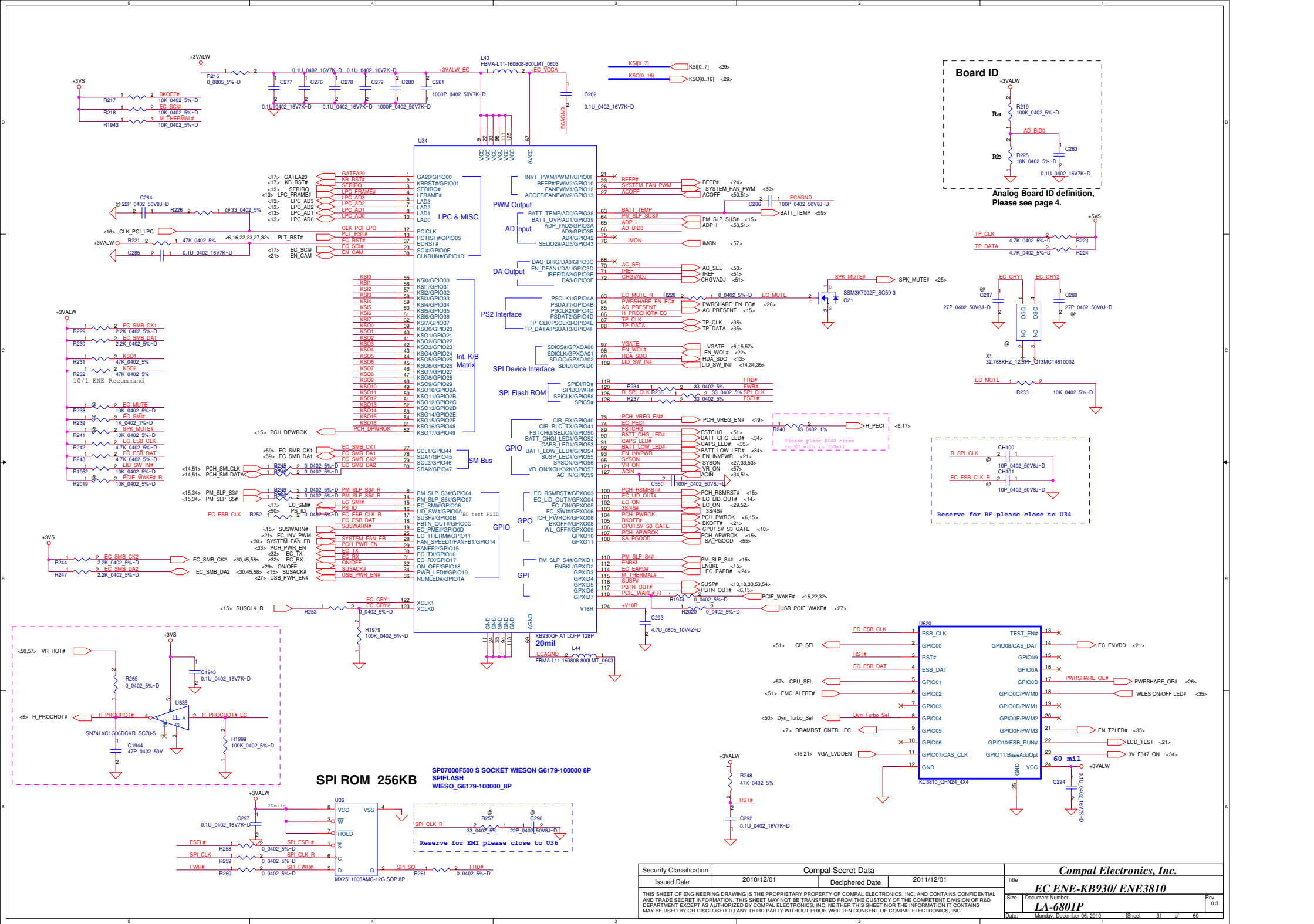


System Thermal Sensor 2

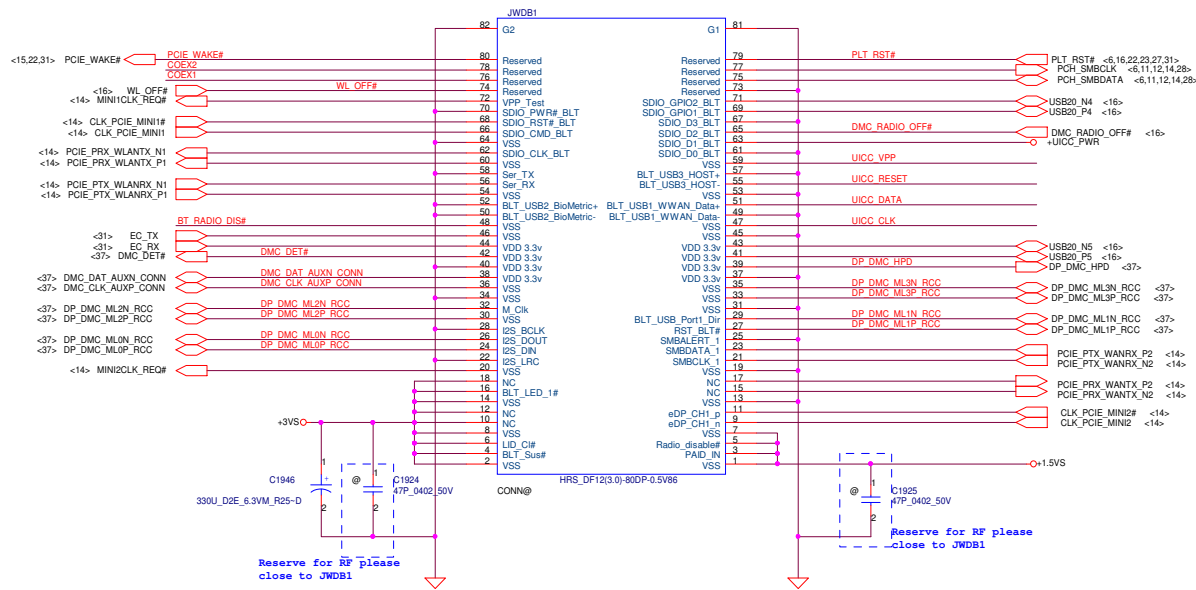
Diode circuit s used for skin temp sensor
(placed around DIMM).
Place C1871 close to Q279 as possible.



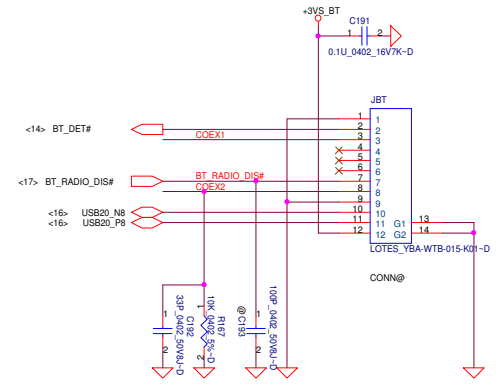
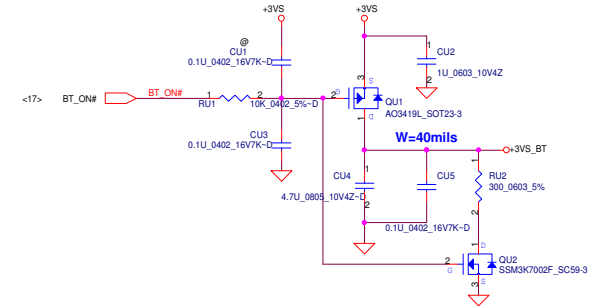
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/12/01	Deciphered Date	2011/12/01	Title	FAN Controller
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				Rev	0.3



To DMC PCB connector

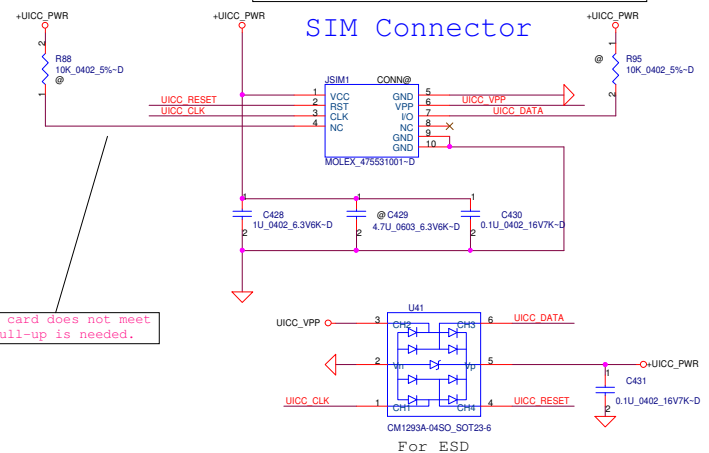


BlueTooth



SIM card board 4.7uF change to 1uF for Tiger detect issue.

SIM Connector

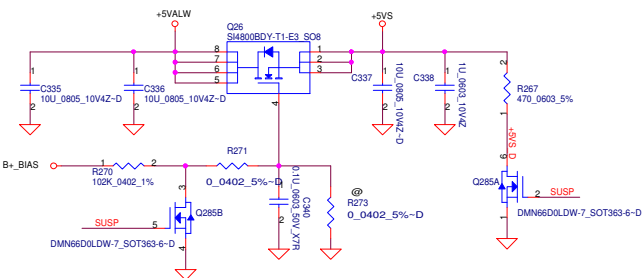


Reserve for SIM card does not meet rise time and pull-up is needed.

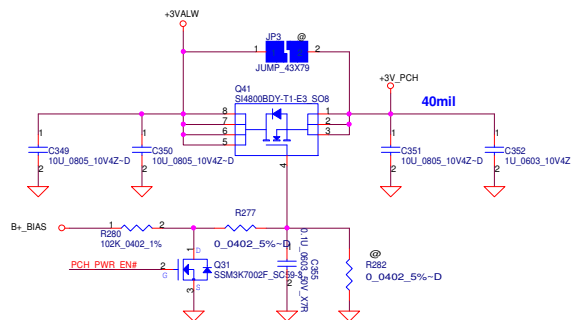
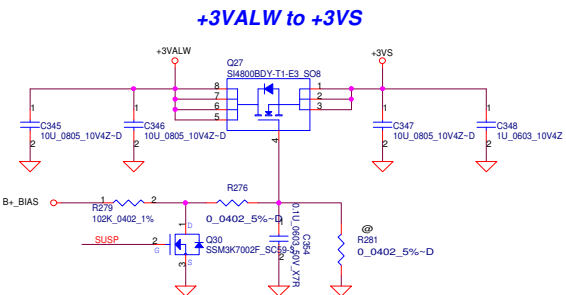
For ESD

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Size	Document Number	Rev	Date: Monday, December 06, 2010	
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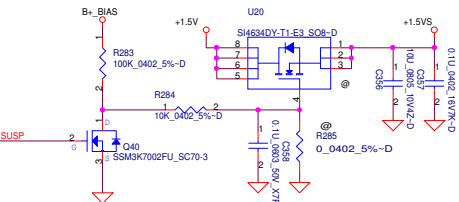
+5VALW to +5VS



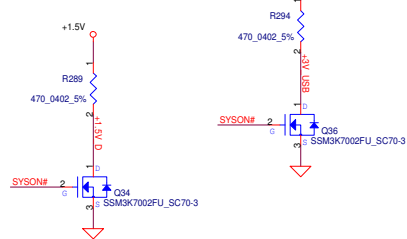
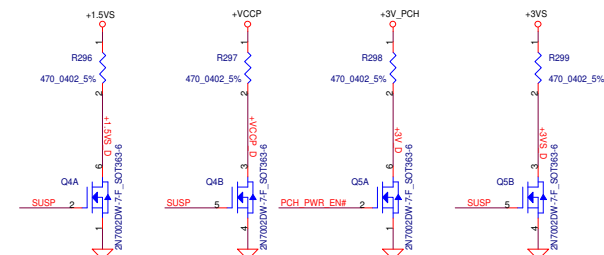
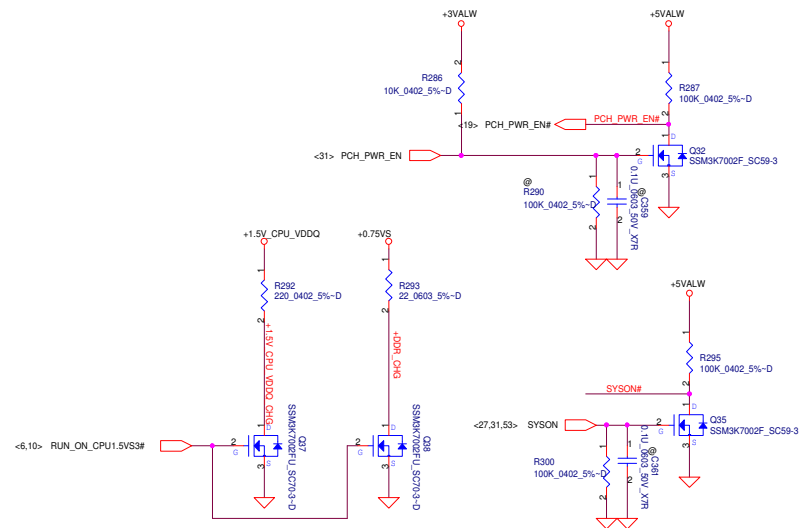
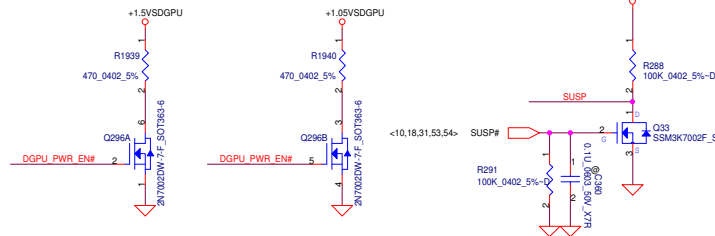
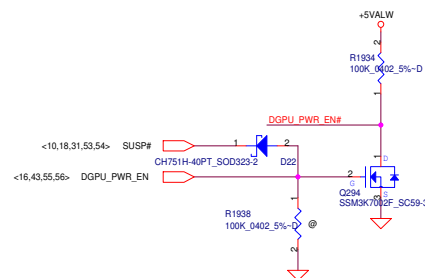
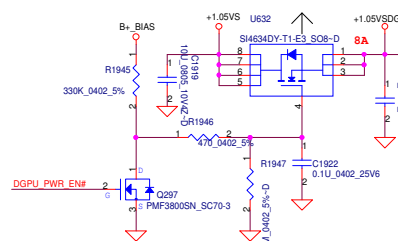
+3VALW to +3V_PCH



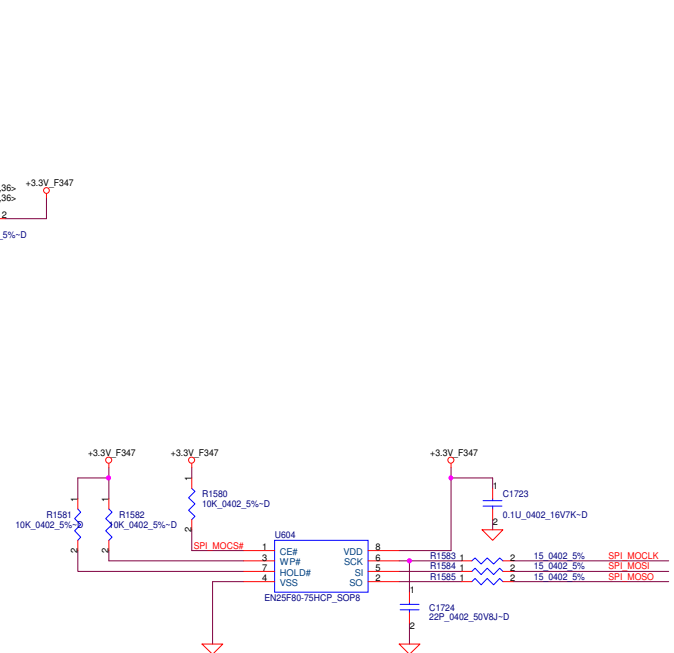
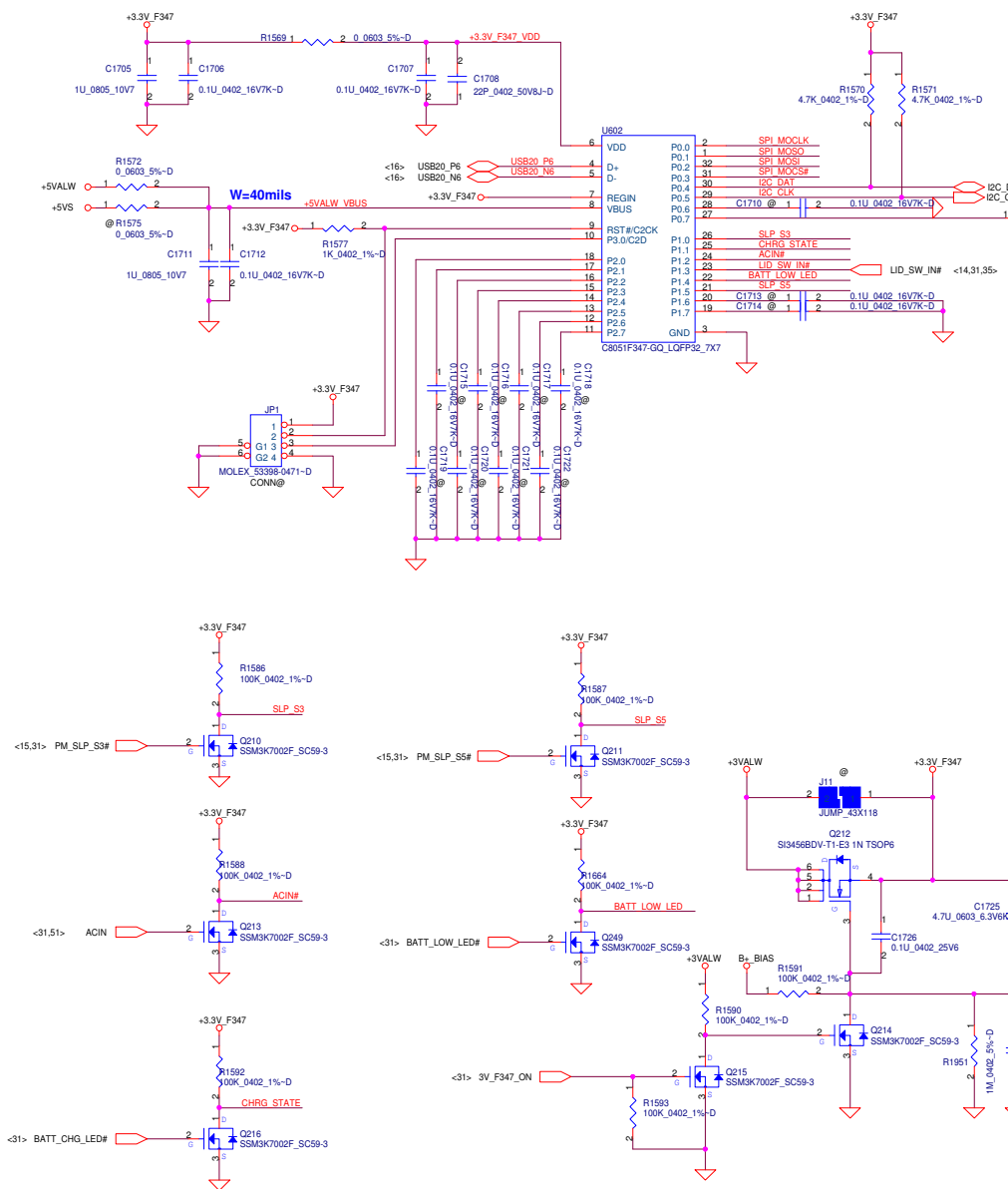
+1.5V To +1.5VS



+1.05V to +1.05VSDGPU Transfer



Security Classification	Compal Secret Data		Title	
Issued Date	2010/12/01	Deciphered Date	2011/12/01	DC/DC Interface
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				Document Number
				LA-6801P
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				0.3
				Date: Monday, December 06, 2010
				Sheet 33 of 60

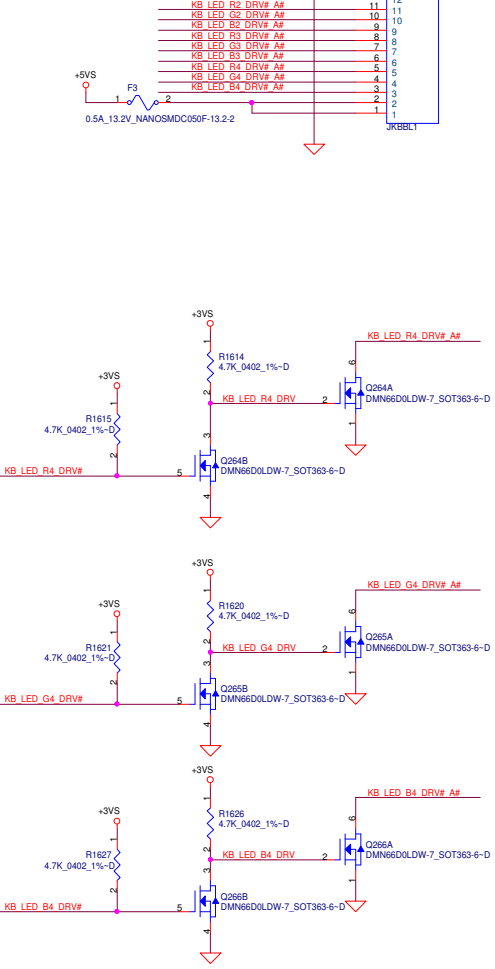
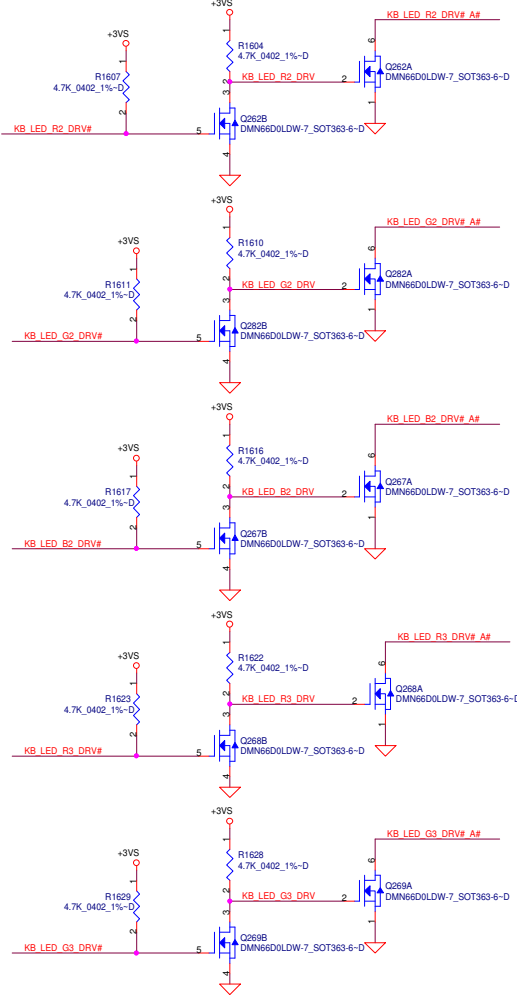
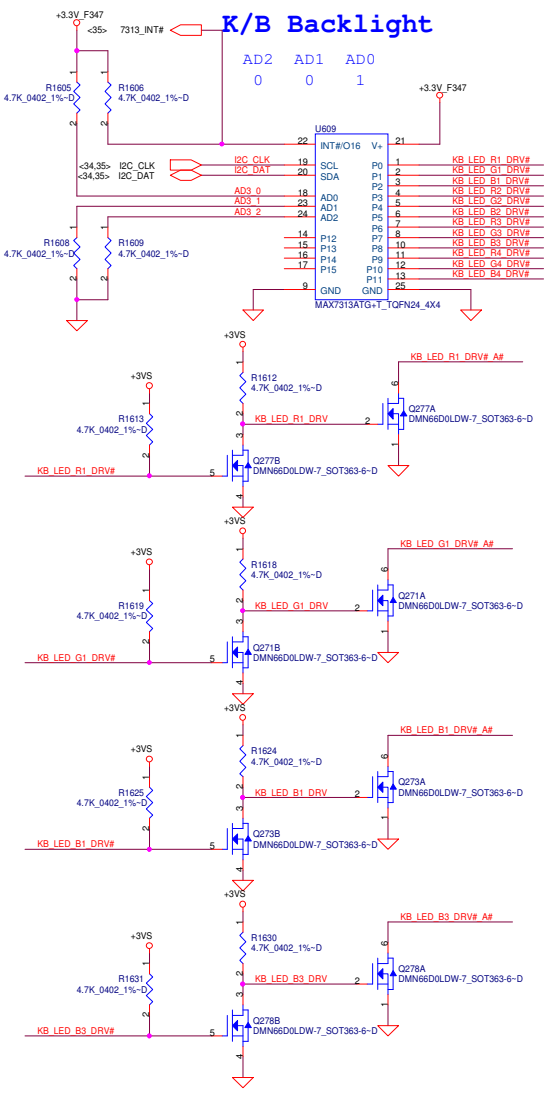


+3.3V_F347 behavior

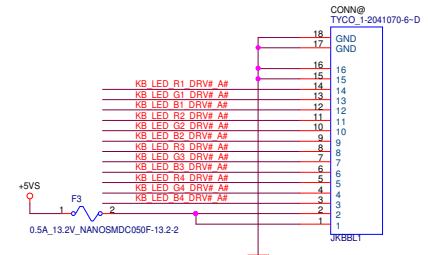
	STATE				
	S0	S3	S4	S5	
AC IN	ON	ON	ON	ON	
BAT only	ON	ON	OFF	OFF	

DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b

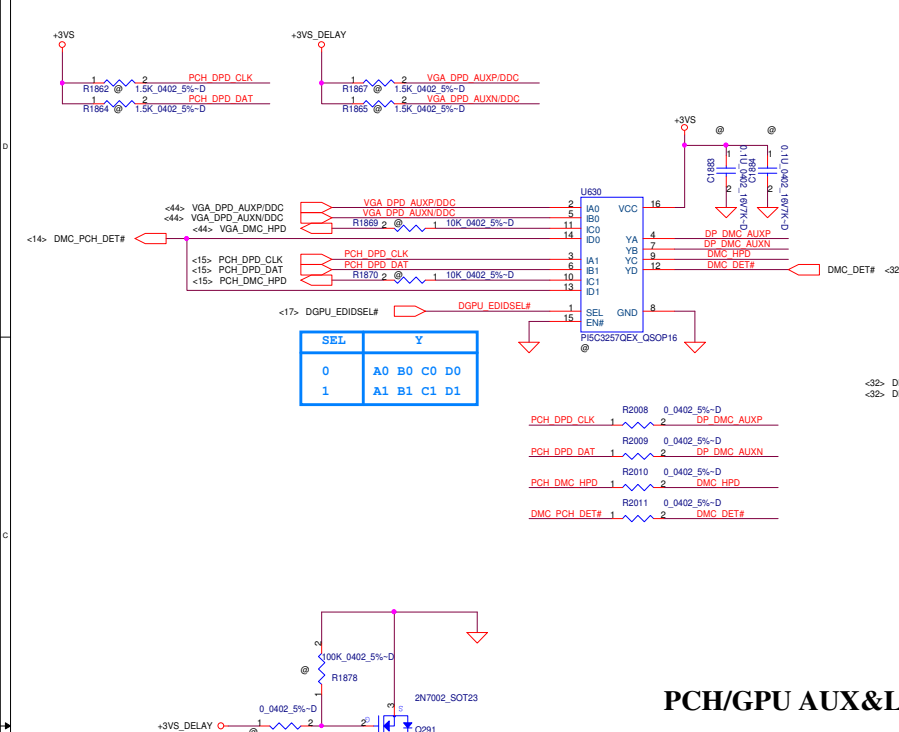
AC mode battery full in S5:turn off ELC controller



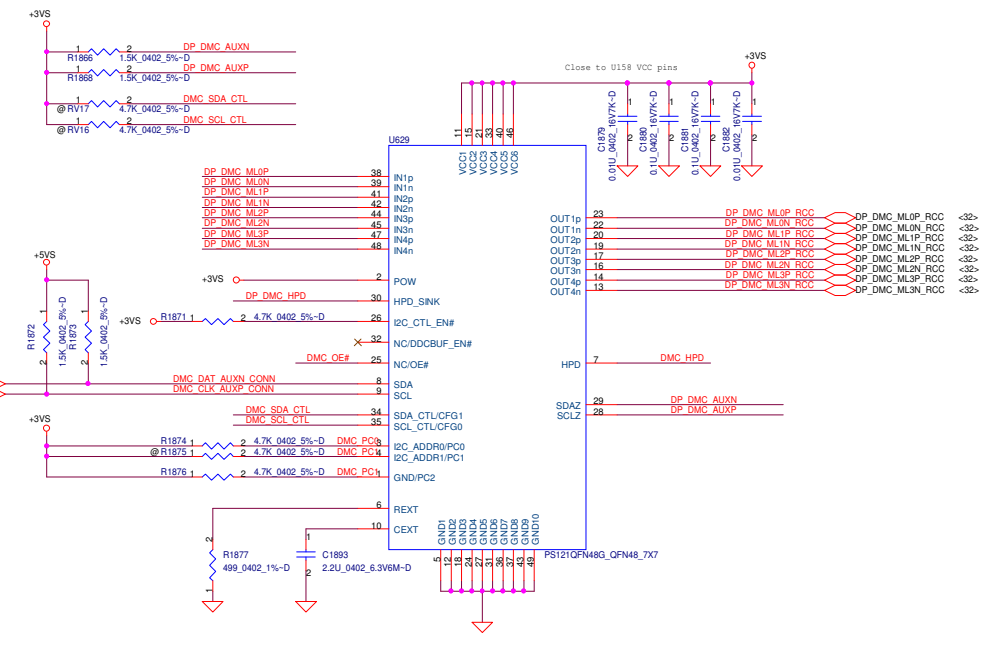
K/B Backlight CONN



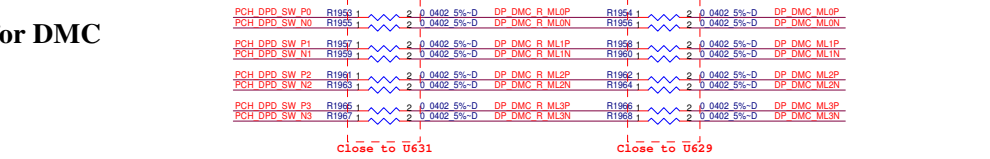
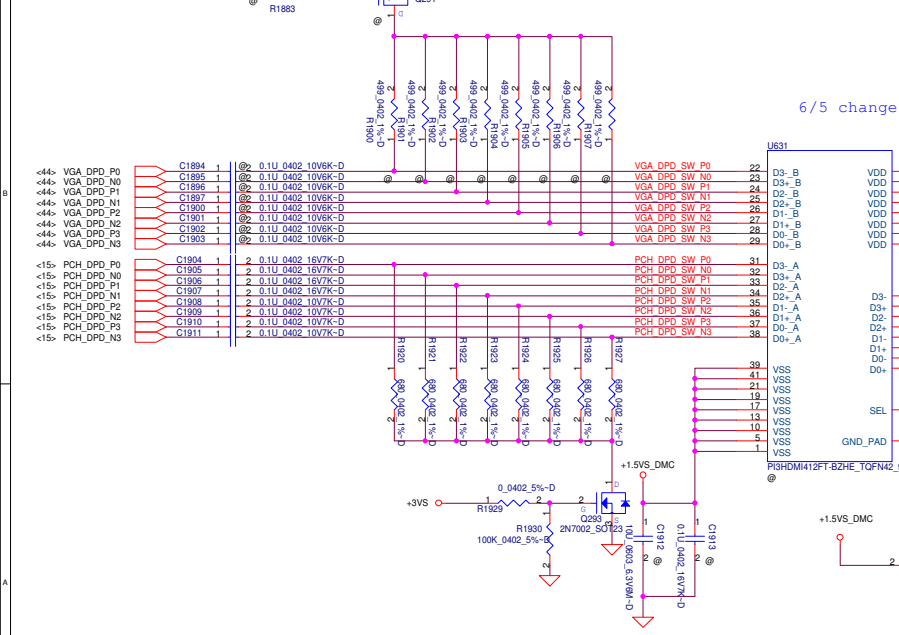
PCH/GPU DDC SW for DMC



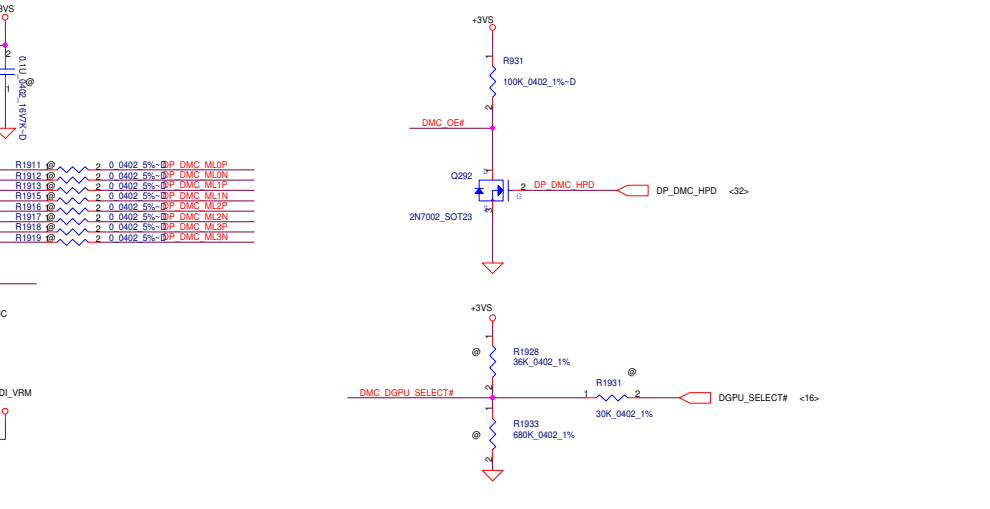
DMC Redriver



PCH/GPU AUX&LANE SW for DMC



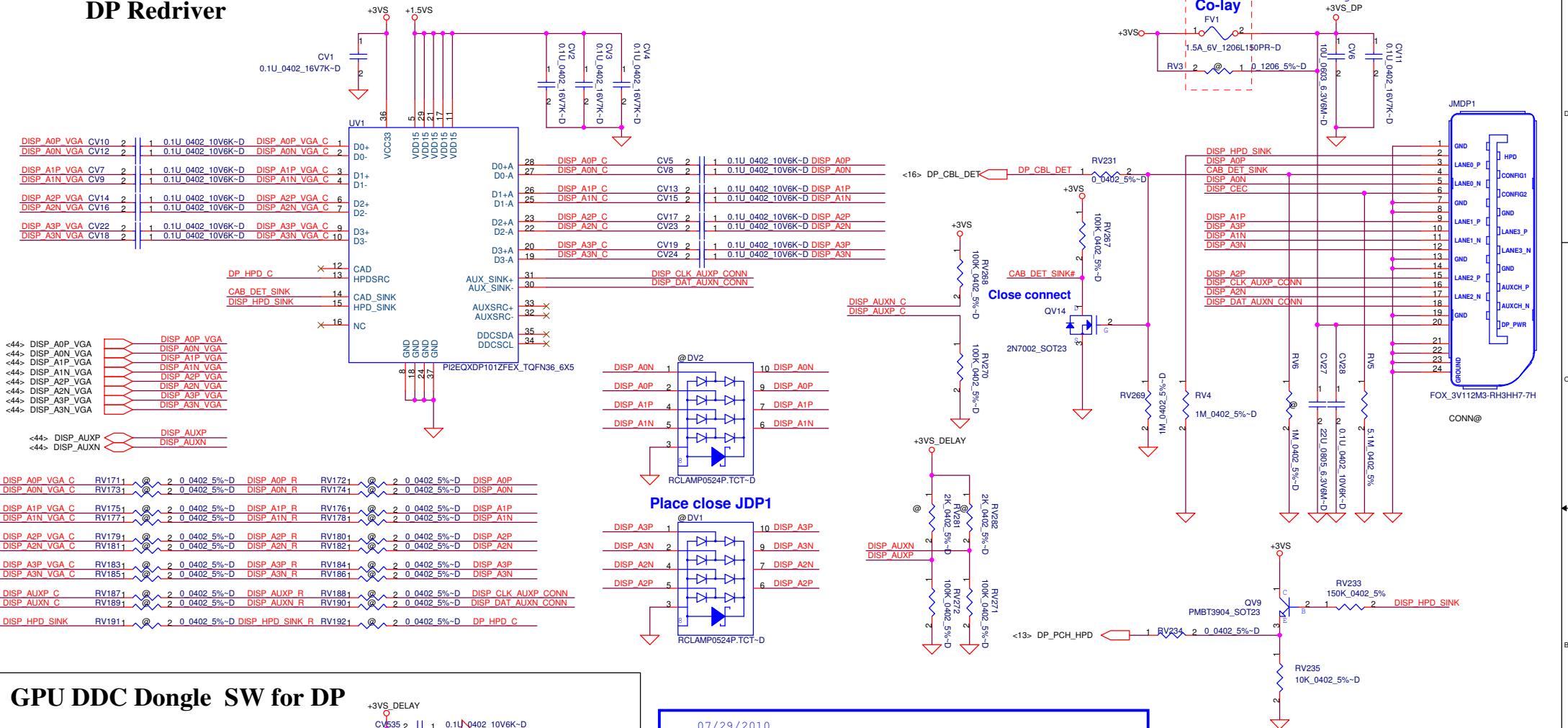
6/5 change C188, C1162 0805 to 0603



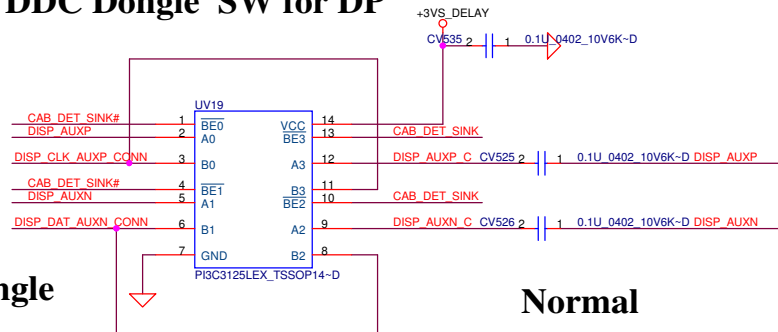
AUX_SEL/SEL1&2	Chanel	Source
0	A	GPU
1	B	PCH

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Issued Date		2010/12/01	Deciphered Date	2011/12/01	Title			DMC MUX/Redriver
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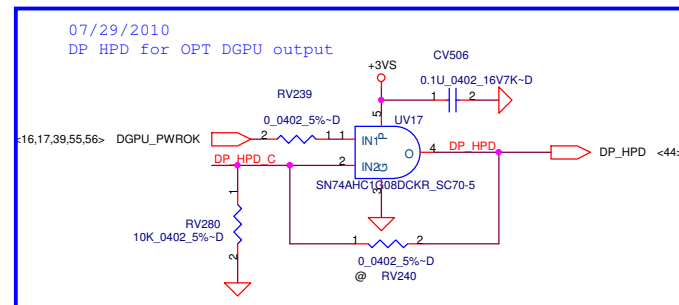
DP Redriver



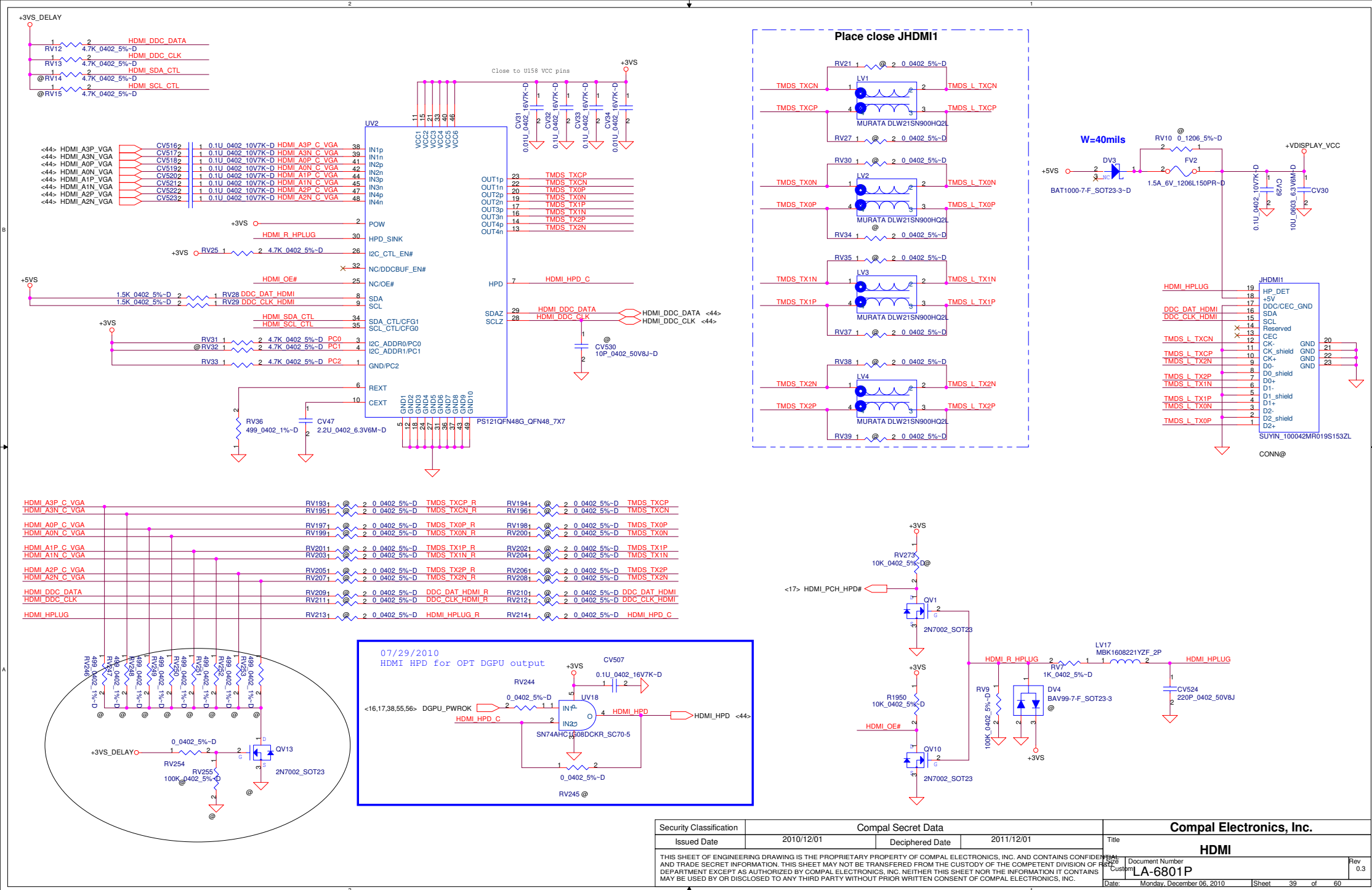
GPU DDC Dongle SW for DP

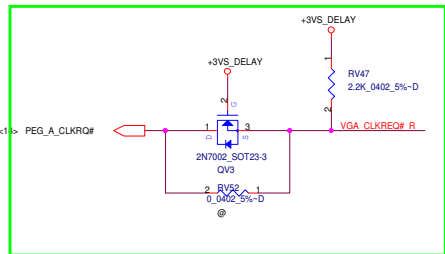
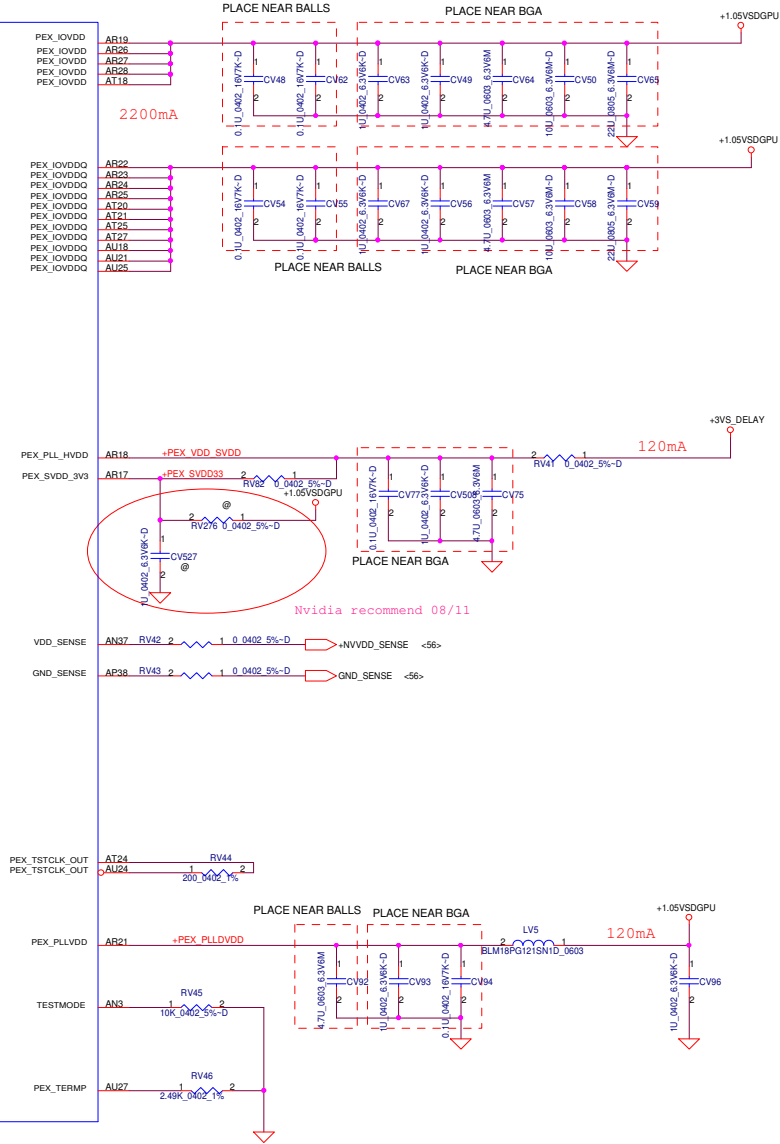
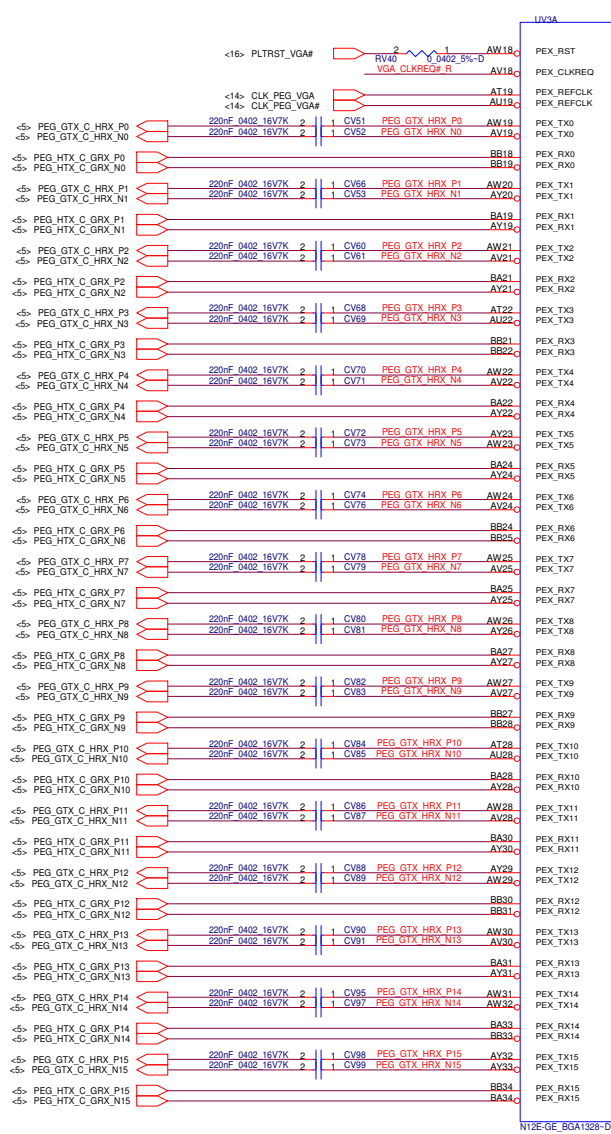


Normal

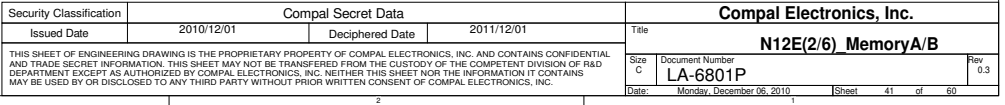


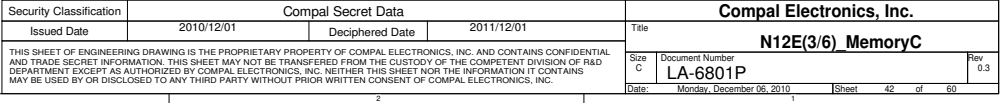
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2010/12/01	Deciphered Date	2011/12/01	Title		
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				Size	Document Number	Rev
				Custom	LA-6801P	0.3
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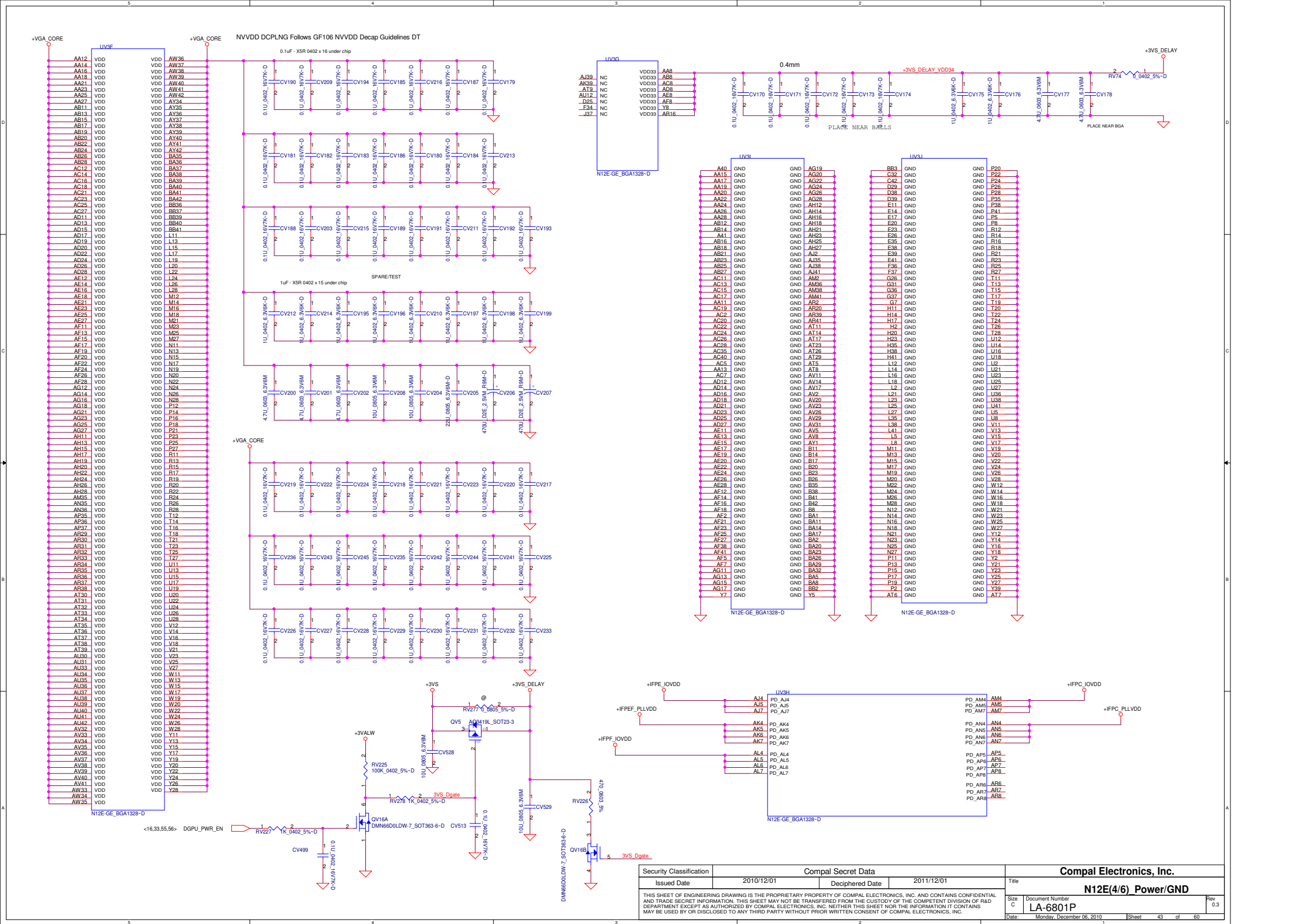


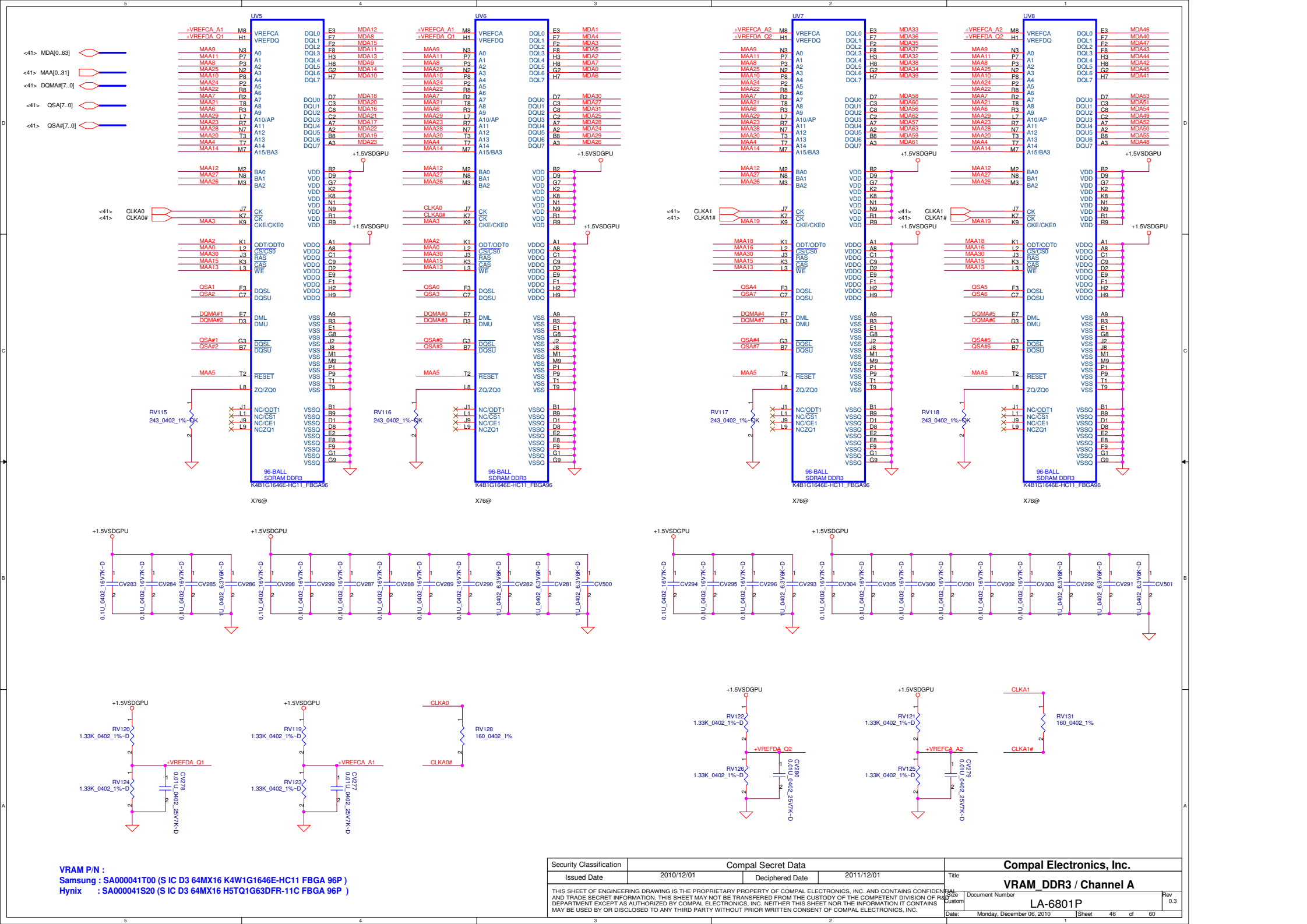


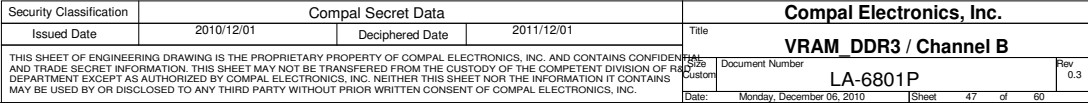
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/12/01	Deciphered Date	2011/12/01	Title
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Size	C	Document Number	LA-6801P	Rev 0.3
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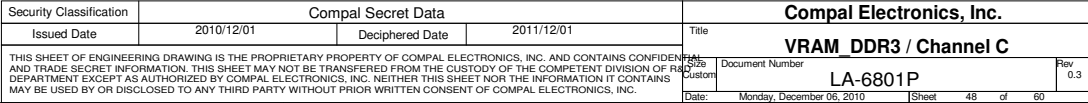




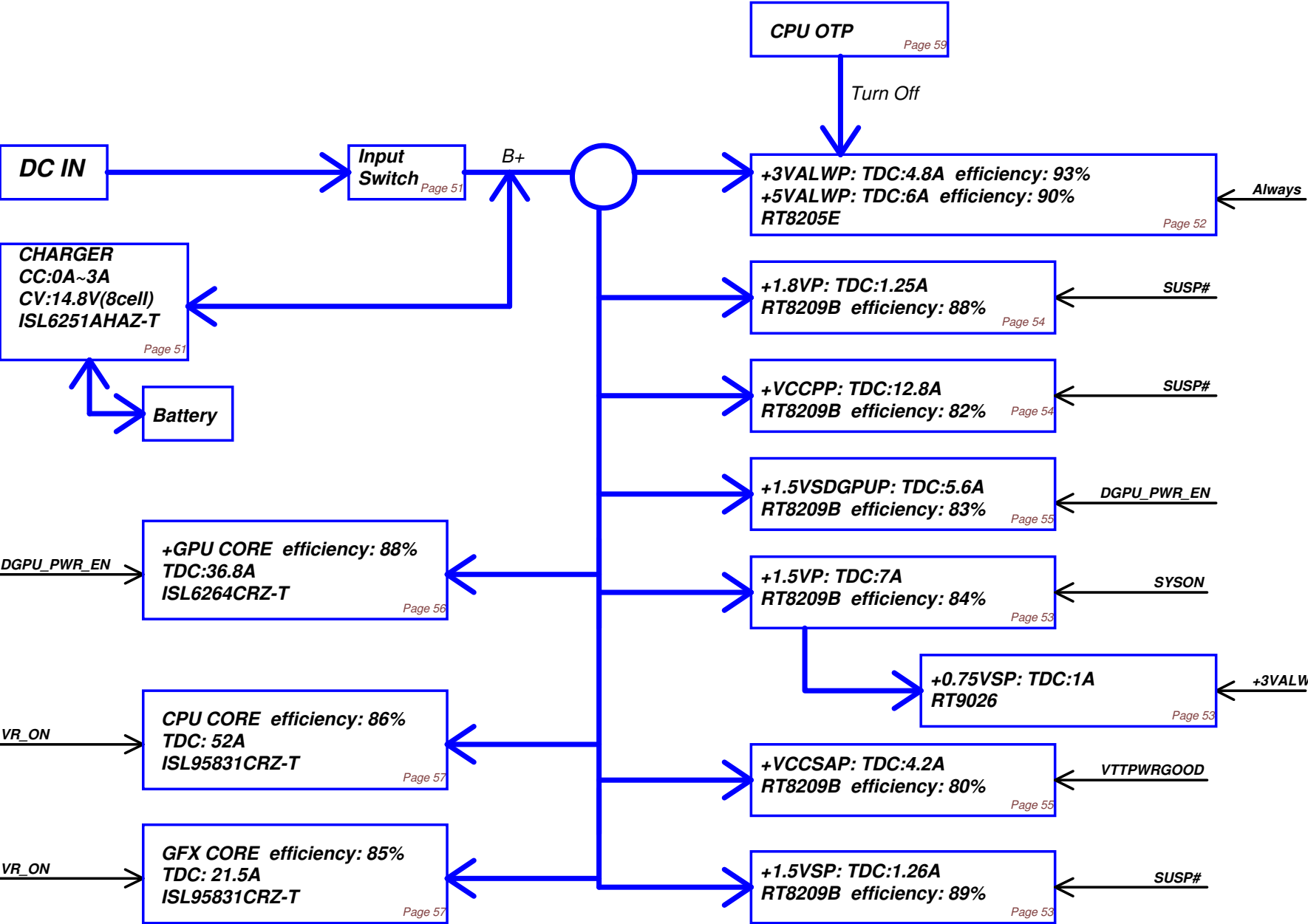


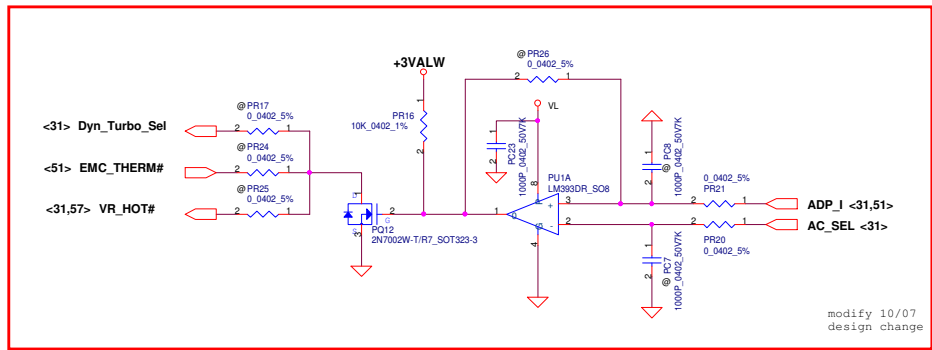






Power block

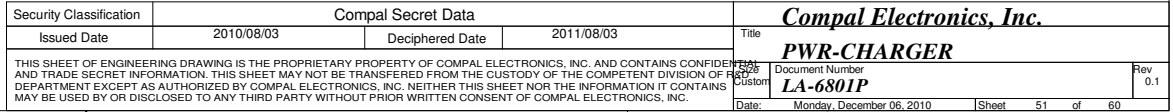




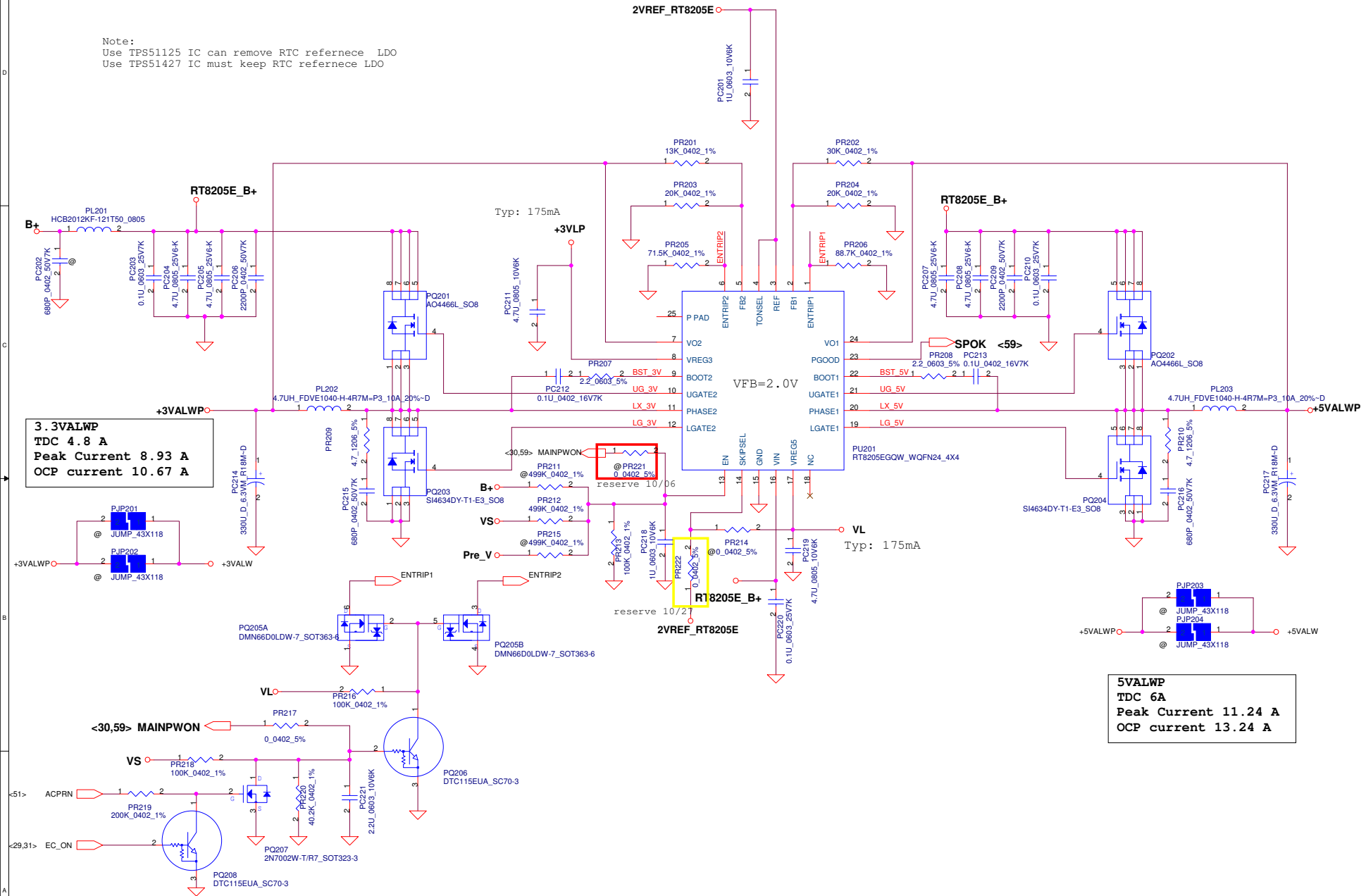
Security Classification	Compal Secret Data		Compal Electronics, Inc. PWR-DCIN / Vin Detector	
Issued Date	2010/08/03	Deciphered Date	2011/08/03	Title
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Date: Monday, December 06, 2010			Sheet 50 of 60	

$$CP = 90\% \cdot I_{ada} ; CP = 6.92A$$

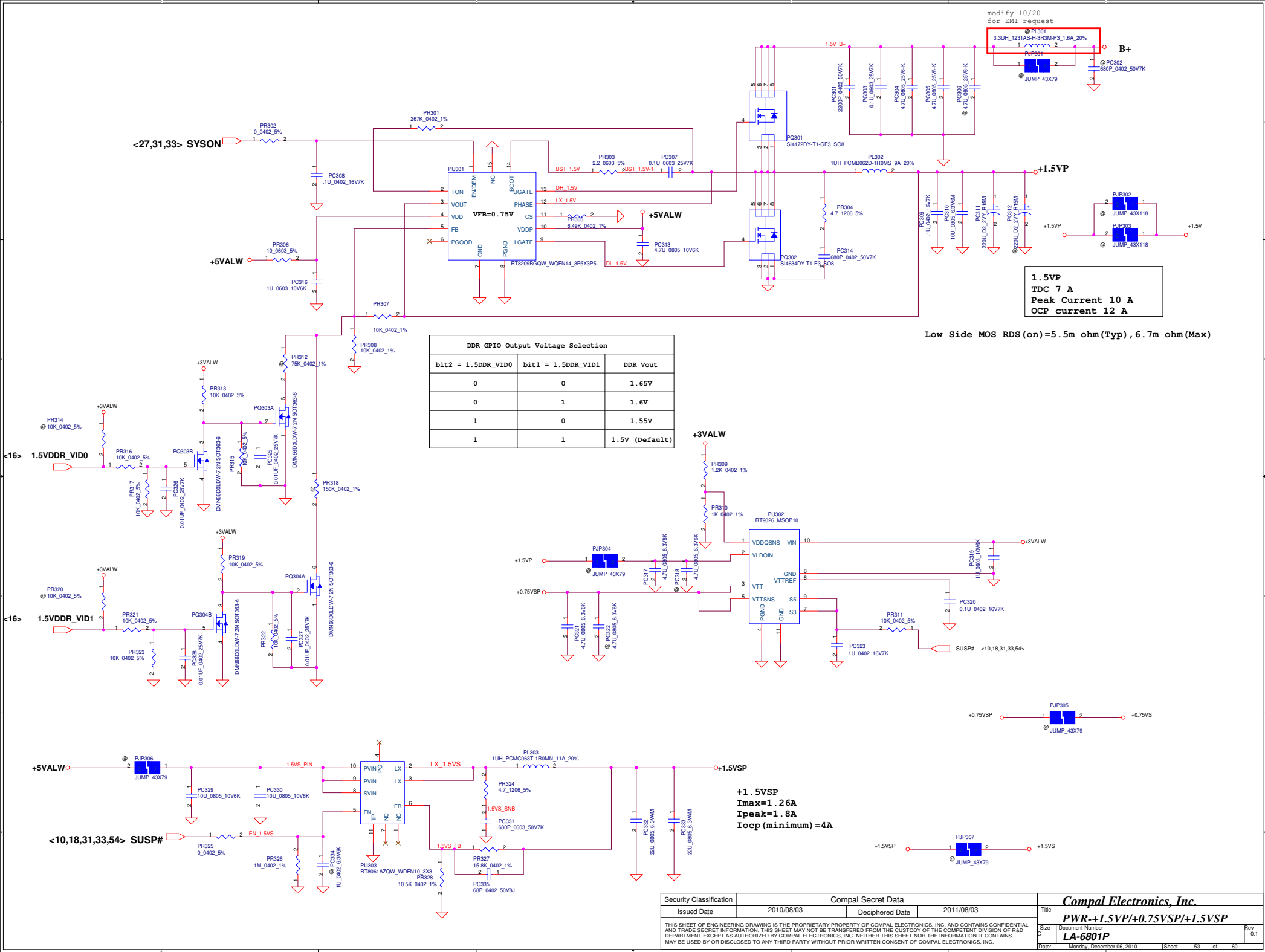
```
add 10/20
for EMI request
```



Note:
Use TPS51125 IC can remove RTC reference LDO
Use TPS51427 IC must keep RTC reference LDO

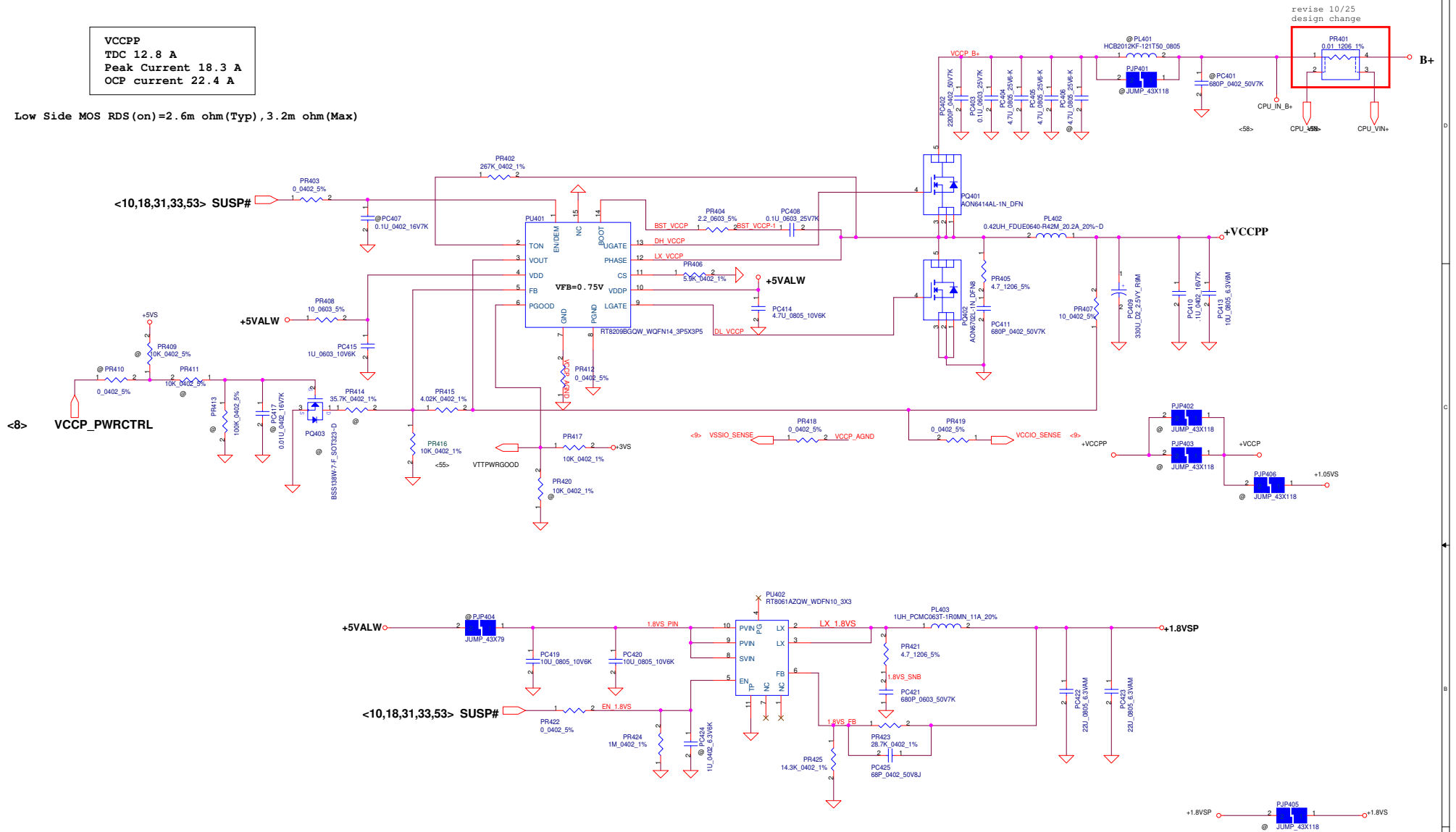


Security Classification	Compal Secret Data			Title	
Issued Date	2010/08/03	Deciphered Date	2011/08/03	3VALWP/5VALWP	
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				LA-6801P	0.1
				Date: Monday, December 06, 2010	Sheet 52 of 60

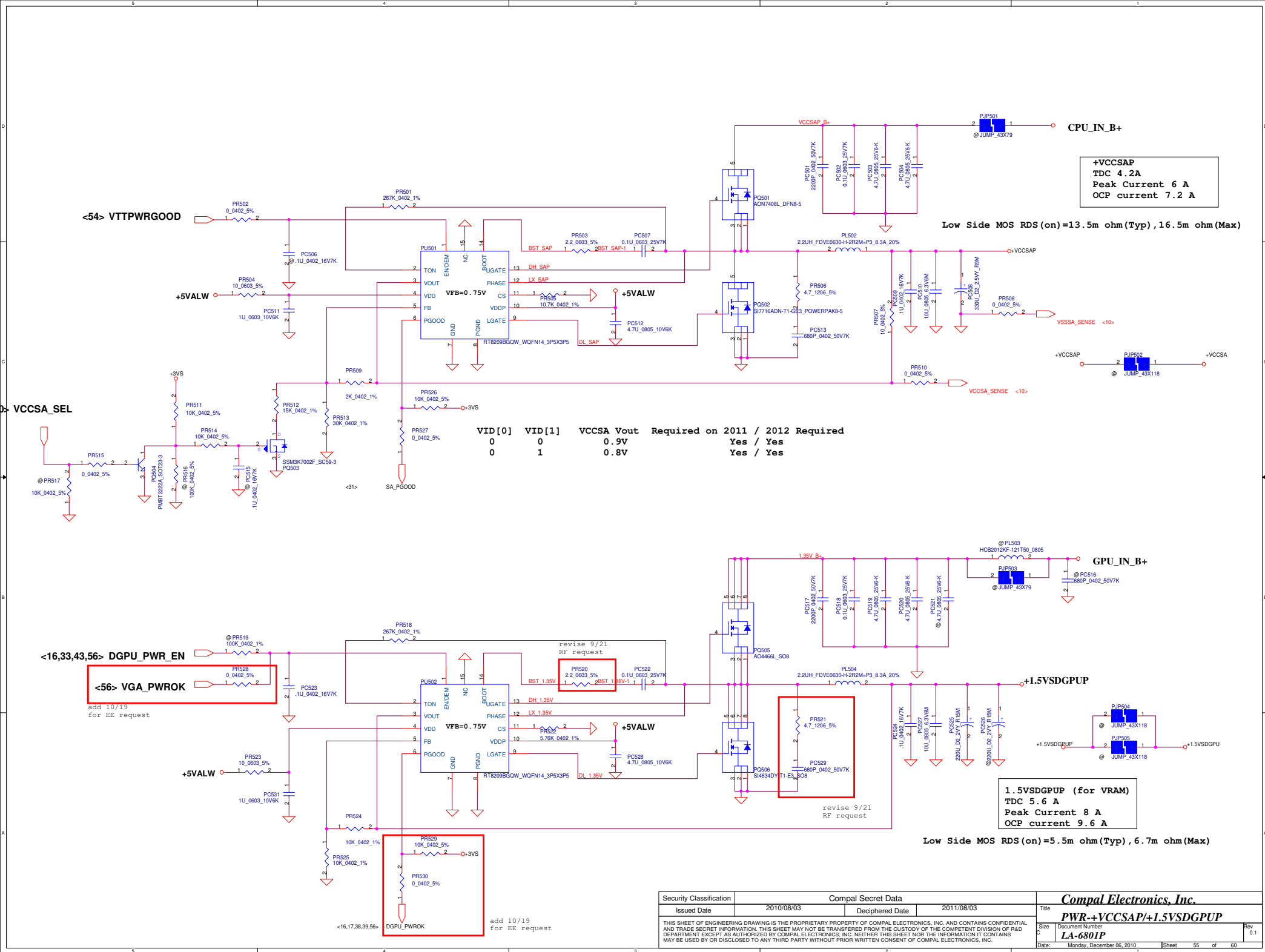


VCCPP
TDC 12.8 A
Peak Current 18.3 A
OCP current 22.4 A

Low Side MOS RDS(on)=2.6m ohm(Typ) , 3.2m ohm(Max)



1.8VSP
TDC 1.25 A
Peak Current 1.75 A
OCP current 4 A



+VCCSAP
TDC 4.2A
Peak Current 6 A
OCP current 7.2 A

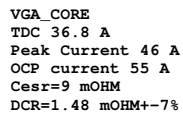
Low Side MOS RDS(on)=13.5m ohm(Typ) , 16.5m ohm(Max)

VID[0]	VID[1]	VCCSA Vout	Required on 2011 / 2012 Required
0	0	0.9V	Yes / Yes
0	1	0.8V	Yes / Yes

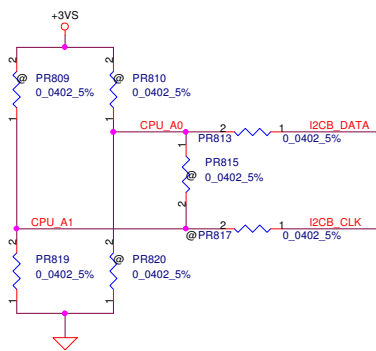
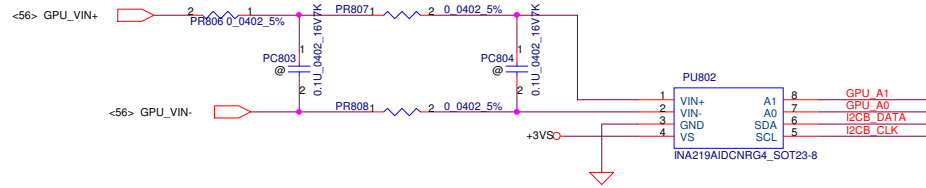
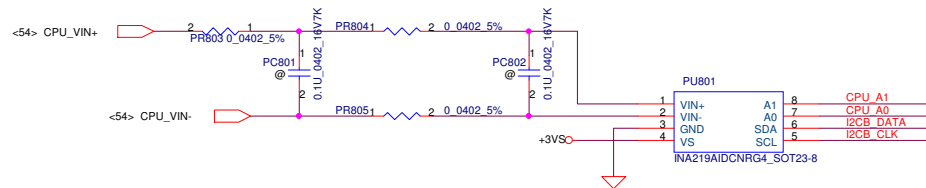
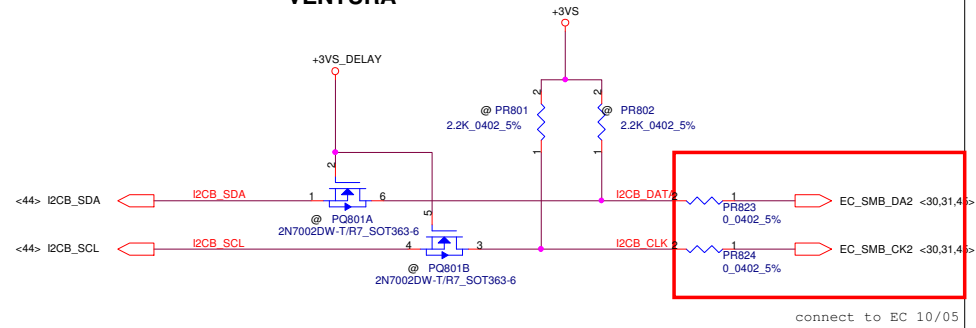
1.5VSDGPUP (for VRAM)
TDC 5.6 A
Peak Current 8 A
OCP current 9.6 A

Low Side MOS RDS(on)=5.5m ohm(Typ) , 6.7m ohm(Max)

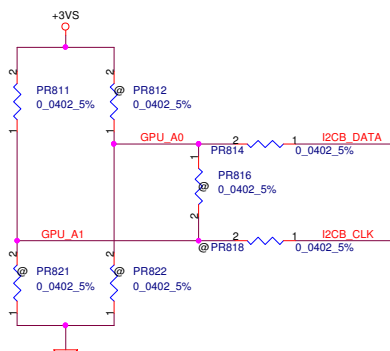
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2010/08/03	Deciphered Date	2011/08/03	Title	PWR-+VCCSAP/+1.5VSDGPUP	
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				Date	Monday, December 06, 2010	Sheet

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VENTURA



Ventura for CPU side
slave address : 1000010
please placemnet near R-sense

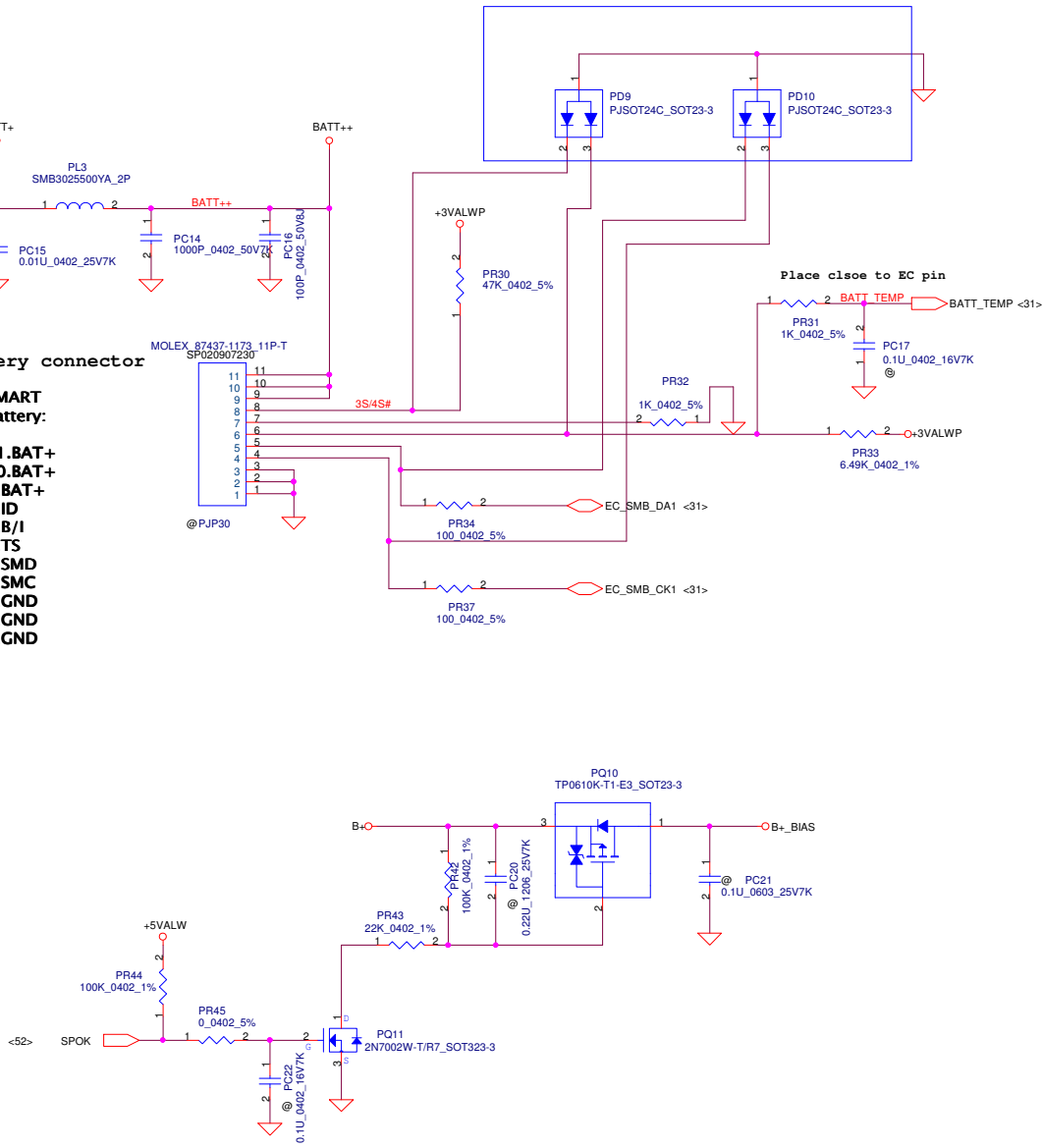


Ventura for GPU side
slave Address 1000110
please placement near R-sense

PJP30 battery connector

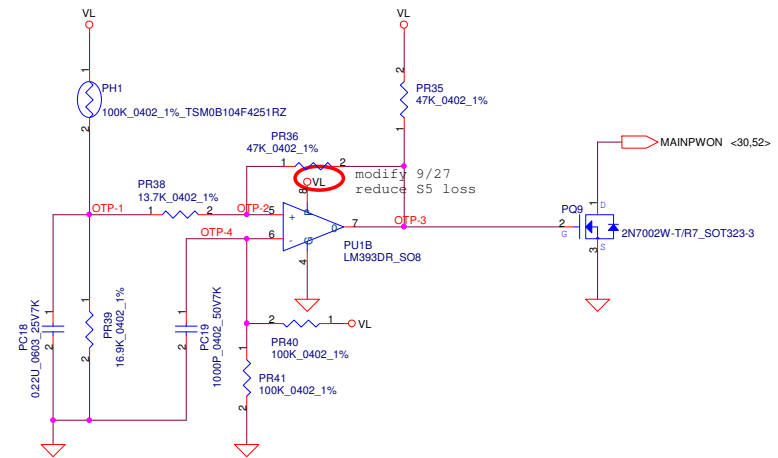
**SMART
Battery:**

- 11.BAT+
- 10.BAT+
- 9.BAT+
- 8.ID
- 7.B/I
- 6.TS
- 5.SMD
- 4.SMC
- 3.GND
- 2.GND
- 1.GND



Battery Connect/OTP

PH1 under CPU bottom side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C



Security Classification		Compal Secret Data		Title	
Issued Date	2010/08/03	Deciphered Date	2011/08/03	PWR-BATTERY CONN	
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Issued Date	2009/10/07	Deciphered Date	2012/09/28	Title	PWR-PIR
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				Date: Monday, December 06, 2010	Sheet 60 of 60

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